A New Differential LNA Topology for Wireless Applications

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ABSTRACT

In this paper a new topology of differential Low Noise Amplifier for wireless applications is presented. This solution allows a drastic area reduction, with respect to traditional emitter coupled topology, since it makes possible to achieve the integrated matching at the input by using only down-bond wiring. In this way no integrated inductors are needed. As shown by simulations, an increased linearity range can also be obtained, without impairing the noise figure.
As an example of this new solution, a LNA has been designed for 2.44 GHz frequency operation. The main characteristic of this amplifier are: a noise figure of 1.56 dB, a voltage gain of 19.5 dB, an input impedance of 50 Ω, an input-referred 3rd intercept point of -7.25 dBm and a dissipated power equal to 19 mW.

1. INTRODUCTION

The Noise Figure (NF), the input dynamic range, the matching of the input impedance to 50 Ω and the dissipated power are the main parameters characterizing a Low Noise Amplifier (LNA) for wireless applications. As for the impedance, it is important to achieve the so called *integrated matching*, that is to obtain the minimum NF and the maximum output power with a 50 Ω source impedence [1]. This can be done by suitably choosing the transistor quiescent point and the values of the inductors L_0 and L_1 in Fig. 1 [1-2]. Unfortunately, the integrated inductors are characterized by a quite low value of their quality factor Q (typically Q is lower than 10), moreover they require a large area occupancy on the die.
The low Q implies a not negligible series equivalent resistance, which impairs the NF, and the large area has a negative impact on yield and cost.
For this reason, whenever it is possible, inductors are realized by exploiting wire bonding [3]. Unfortunately, this solution can be adopted only when the inductors are connected in series with an external lead or with the back grounded plane. This is not the case of classical Emitter Coupled Differential (ECD) input stage.
In this paper a new topology of differential LNA, named Base Coupled Differential (BCD), is presented. With respect to ECD, the new topology allows a reduction of the die area and an increase of the dynamic range without causing any performance degradation in terms of NF, dissipated power and gain.

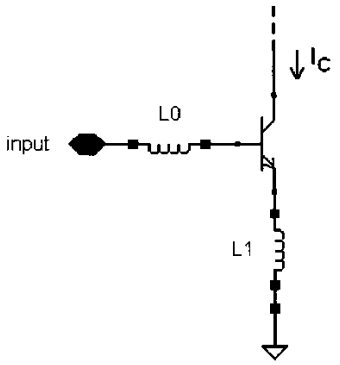

Figure 1. Input matching technique

2. BASE COUPLED DIFFERENTIAL AMPLIFIER

The proposed BCD amplifier is shown in Fig. 2, where some details are omitted for sake of clarity.

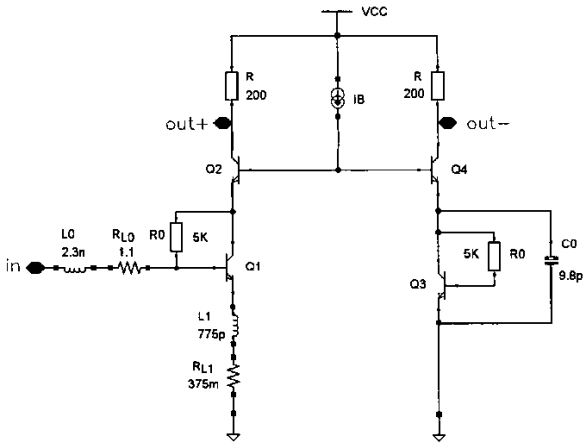

Figure 2. Base Coupled Differential (BCD) amplifier.

Particularly, I_B represents a dc current source implemented by a current mirror scheme. L_1 is realized by means of down-bonding wire to the ground plane and L_0

is obtained by using bonding wire to the input pad: both of them are necessary to obtain the integrated input matching. The Q values for the wire bonding inductors have been estimated in 30. For small signals, $i_{b2} = - i_{b4}$, where i_{b2} and i_{b4} are the small signal base current variations of Q_2 and Q_4 respectively. At low frequencies, at which the effects of the intrinsic capacitances of the transistors are negligible, $i_{b2} = i_{e2}/(h_{fe2} + 1)$ and $i_{b4} = i_{e4}/(h_{fe4} + 1)$. Here, i_{e2} and i_{e4} are the small signal variations of the emitter current while h_{fe2} and h_{fe4} are the current gain, of Q_2 and Q_4 respectively. In the ideal case $h_{fe2} = h_{fe4}$, then the variations of the emitter currents of the two transistors and, consequently, those of the respective collector currents, have the same magnitude, but opposite sign. Therefore, a perfectly symmetric output is obtained and the amplifier realizes the transition from a single-ended input to a differential output in an ideal way.

The shunt capacitor C_0 has been introduced to reduce the input impedance seen at the base of Q_4. At high frequencies, its effect is very important to obtain the opposite values of the collector currents of Q_2 and Q_4.

SpectreRF simulation results have shown that a slight unbalancing of the output voltages Vout+ and Vout- (due to the residual unbalancing between the two emitter impedances) can be completely recovered, up to several GHz, by adding a very small capacitance (62 fF, not shown in Fig. 2) between the collector and the base of Q_2. A quite good symmetry of the two outputs with respect to ground, around the operating frequency of 2.44 GHz, has been obtained in such a way.

3. DIFFERENT TOPOLOGIES: SIMULATION RESULTS

A comparison against the widely [4] used differential cascode configuration, shown in Fig. 3, and here named Cascode Emitter Coupled Differential (CECD) has been carried out. In both cases a single-ended input signal has been considered.

The inductors (L_0, L_1 and L_2) realize the integrated matching. L_0 can be implemented by a bonding wire plus a microstrip while L_1 and L_2 have to be integrated on chip. The parasitic series resistance of L_0 has been calculated by considering a quality factor Q nearly equal to 30. For the on-chip inductors, L_1 and L_2, a value of Q = 8 has been considered, while the area size is of about 100 µm x 100 µm each, as shown in [5]. One of the negative aspects of this configuration is the reduced linearity, if compared with a single-ended cascode amplifier (as the BCD). In fact, Meyer has demonstrated in [6] that, at a fixed dissipated power, the differential pair transconductance stage exhibits an Input-referred 3rd order Intercept Point (IIP_3) about twice lower than that of the common emitter stage.

Since the most significant parameters of a LNA are the NF and the gain at 50 Ω of source impedance, the biasing point has been chosen in such a way to obtain the same NF (which, in this case, is very close to the minimum NF of the transistors).

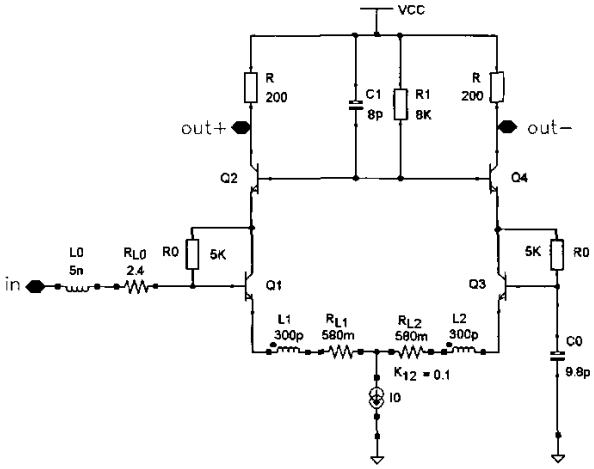

Figure 3. Cascode Emitter Coupled Differential (CECD) amplifier.

Therefore, in both of the cases, the integrated matching has been realized. Moreover, gain and output impedance are the same for both configurations.The amplifiers have been designed by using the HSB3 (High Speed Bipolar) bipolar process by ST Microelectronics. It is a Polysilicon Self-Aligned process (with three levels of metals) for RF applications, with 50 GHz of cut-off frequency.

The simulations results have been performed by means of SpectreRF, a commercial RF analog circuit simulator integrated within the Cadence Design framework. Periodic Steady State analysis has been utilized to predict the 3rd Intercept Point (IP_3) and the 1dB Compression Point (CP_{1dB}). The best results obtained for each configuration are reported in Tab. A and discussed in Section IV.

The IIP_3 has been evaluated considering two input tones at frequencies f_1 = 2.432 GHz and f_2 = 2.448 GHz. In agreement with [6], the 1 dB Input Compression Point (ICP_{1dB}) was approximately 9.6 dB lower than IIP_3 for all the considered configurations, so it is not reported in Tab. A. The load impedance between Vout+ and Vout-, not indicated in Figs. 2 and 3, has been considered equal to 1 kΩ.

Fig. 4, a) and b), shows the layouts of the BCD and the CECD amplifiers, respectively. In both of them, BP is the ground shielded pad connected to the base of the input transistor Q1; in a) EP is the ground shielded pad connected to the emitter, of the input transistor Q1, which has to be down bonding wired to the back grounded plane.

Clearly, the area required by the ECD is larger mainly due to the integrated inductors. The area size (h x w product) reported in Tab. A does not include the contributions of the capacitor C_0 and of the output buffer stage, but only

the contribution of the amplifier itself has been considered.

	BCD	CECD
NF [dB] (*)	1.56	1.78
A_V [dB] (*)	19.5	19.5
Z_{in} [Ω] (*)	50	50
P_D [mW]	19	21.3
IIP_3 [dBm] (*)	-7.25	-8.8
IS [dB]	-53.9	-54.9
PSRR [dB] (*)	21.55	10.97
Area [mm^2]	0.027	0.077
Down Bond	yes	No

Table A : Simulation results; A_v is the forward voltage gain (V_{out} / V_{in}); IS is the reverse voltage gain (V_{in} / V_{out}) evaluated at 2.54 GHz; PSRR is the ratio A_V/A_{CC}, where A_{CC} is $V_{out}/\Delta V_{CC}$ at 2.44 GHz.

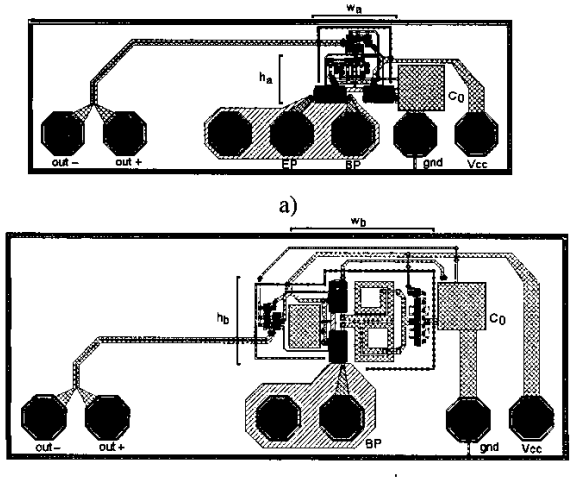

Figure 4. a) BCD layout: total area (double trench included) = 404 x 1260 μm^2; h_a = 125 μm, w_a = 215 μm; b) ECD layout: total area = 574 x 1430 μm^2; h_b = 205 μm, w_b = 375 μm.

4. COMPARISONS AND DISCUSSION

The main parameters in Tab. A, which have been considered for the comparison are: the dissipated power P_D, the IIP_3, and the area size. As far as P_D is concerned, it is worth noting that, in the CECD configuration, the total current is greater that I_0. Indeed, in Fig. 3 the biasing circuitry is not represented. The current I_0 has been obtained by using a current mirror realized by means of two transistors whose area ratio is 1/6, so that, in this way, the total current supplied by the batteries is $I_0 + I_0/6$.

Other parameters to be considered are Isolation (IS) and Power Supply Rejection Ratio (PSRR). The former is defined as the ratio V_{in} / V_{out} (measured by supplying the output with a small signal and by shunting the input with a 50 Ω resistor), which gives a measurement of the possible effects of the local oscillator to the input (oscillation frequency has been considered equal to 2.54 GHz). PSRR is the ratio A_V/A_{CC}, where A_{CC} is the ratio between the output voltage and the an eventual disturb superimposed to the power supply.

The comparison between BCD and CECD configurations shows the superiority of the BCD. Particularly, two are the main advantages of the BCD: (i) the smaller area size and (ii) the higher IIP_3.

The former advantage (i) does not require any further clarification: a comparison among the layouts reported in Fig. 4 clearly shows the negative impact on the area occupancy of integrated inductors: the product w x h is nearly 3 times larger that one of the BCD solution. The latter advantage (ii) derives from the single-ended input which permits to obtain a larger linearity range, according to Meyer's demonstration [7]. This is clearly validated by the data reported in Tab.A showing that BCD is characterized by the highest value of IIP_3.

5. CONCLUSIONS

In this paper we have presented the Base Coupled Differential (BCD) as a bipolar amplifier topology which allows to realize an integrated matching on a single-ended input and provides a differential output. No integrated inductors are needed but down-bonding wire is used to realize the emitter inductive degeneration.

The symmetry of the output voltages with respect to ground has been demonstrated and it has been confirmed by simulation results.

A detailed comparative analysis with the classical Cascode Emitter Coupled Differential configuration has been performed. The results are: an area complexity approximately three times smaller, a better Noise Figure (NF) and Power Supply Rejection Ratio and an increased linearity range.

Moreover, it is worth mentioning that BCD overall performances are among the best reported in literature [8-10] in the last years in bipolar technology, particularly as far as NF is concerned.

This scheme has been employed to realize a LNA in a 2.44 GHz RF front-end for Wireless Local Area Network (WLAN) applications which has been manufactured by STMicroelectronics. The chip has been packaged in a TQFP 48 with exposed pad and will be characterized in Q2/2002.

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