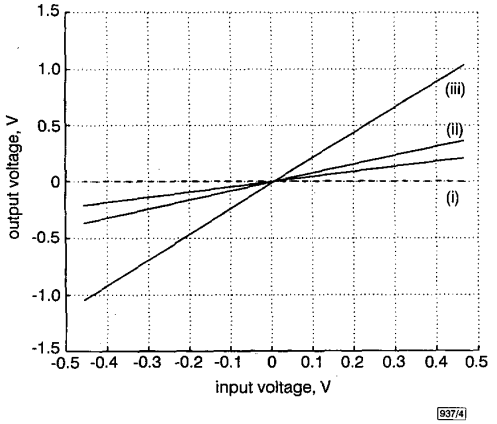

Fig. 4 *Output voltage against input voltage of VGA circuit for different gain settings*

(i) gain = 12
(ii) gain = 18
(iii) gain = 46
– – – linearity error

The gain control step size is found to vary slightly between 0.55 and 0.59dB over the 25dB gain range. These values agree well with the step size of 0.56dB predicted by eqn. 4. To measure the linearity of the VGA the input voltage is swept and the output voltage is plotted for different gain settings. The result is shown in Fig. 4. The linearity error for one of the gain settings is shown by a dotted line and found to be < 0.04% which corresponds to ~11 bits of linearity. The three solid lines are for gain control words 12, 18 and 46, respectively. The input referred noise of the VGA is 21nV/√Hz at 12dB gain setting. The circuit consumes 387μA of standby current from a 3V supply. The bandwidth of the different components of the circuit was measured. The CDN exhibits a bandwidth of > 18MHz, the first amplifier exhibits a bandwidth of 13MHz when current driven by the CDN. Finally the whole VGA has a bandwidth of ~4.1MHz at unity gain.

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H. Elwan and M. Ismail (*Analog VLSI Lab, Department of Electrical Engineering, The Ohio State University, USA*)

A. El Adawi and A. Soliman (*Electronics and Comm. Department, Cairo University, Egypt*)

H.K. Olsson (*Radio Electronics Laboratory, Royal Institute of Technology, Kista, Stockholm, Sweden*)

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High-quality active inductors

G. D'Angelo, L. Fanucci, A. Monorchio, A. Monterastelli and B. Neri

A high-quality active integrated inductor is presented. The circuit has an inductance of 20nH and a quality factor of 47 at 1.8GHz. It is designed to be realised using standard silicon bipolar technology and consumes 2.6mW at a supply voltage of 3V.

Introduction: The design of fully integrated tranceivers for mobile communication systems in the RF band entails the realisation of high quality inductors built on standard silicon technologies to avoid extra processing steps. To increase the quality factor, many techniques have been presented, from the shunt connection of all available metallisation layers [1], to the introduction of *pnp* junctions underneath the inductor to reduce substrate losses [2]. Nevertheless, it is not easy to obtain quality factors greater than 8 for inductors of a few nanohenries; moreover, the achievable values of Q decrease as the inductance rises. In [3] a promising CMOS technique based on an active gyrator was presented. Results showed the possibility of separately regulating the inductance and Q values for frequencies up to 1GHz. Kuhn *et al.* [4] have suggested a novel technique in which an active device is used to implement a negative resistance, to compensate for the losses in the integrated inductor. This method, however, does not provide any increase in the inductance value and may lead to instability.

The circuit concept presented in this Letter provides 20nH of inductance and a peak Q (defined as the ratio between the imaginary part and the real part of the inductor impedance) greater than 45 at the working frequency of 1.8GHz.

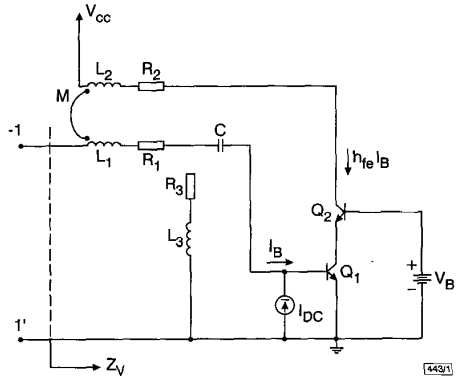

Fig. 1 *Basic principle of inductor*

Circuit design: The active inductor exploits the magnetic coupling between two spiral inductors (L_1 and L_2 in Fig. 1) to increase the inductance value seen at the input terminals. The current across L_1 is amplified by the cascode stage and driven into L_2. The magnetic coupling results in an increase in the voltage drop on L_1 by the factor $j\omega Mh_{fe}i_b$, where M is the mutual inductance between L_1 and L_2 and h_{fe} is the current gain of the cascode. The third inductor L_3 the input resistance and the emitter junction capacitance of Q_1 realise a shunt LRC filter, the resonant frequency of which has to be chosen according to the desired operating frequency. The input impedance of the circuit is expressed by the following formula:

$$Z_V = [R_1 - \omega \cdot M \cdot h_{fe} \cdot \sin\varphi] + j\omega \cdot [L_1 + M \cdot h_{fe} \cdot \cos\varphi] \quad (1)$$

where R_1 is the parasitic series resistance of L_1 and φ is the angle between the current flowing through L_1 and that through L_2; it should be noted that φ depends on the resonant frequency of the L_3RC filter. As the formula predicts, the quality factor of the resulting inductor is high, since the imaginary part of Z_v increases and the real part decreases. Moreover, control of the angle φ, achieved by tuning the bias voltage of the common-base bipolar junction transistor (BJT) Q_2, and control of the current gain h_{fe}, obtained by varying the bias current of Q_1, allows the differences in the circuit response due to process tolerances or thermal excursions to be compensated for. These controls may also be exploited for the design of voltage-variable inductors for VCOs.

Layout: The active inductance has been designed to be realised on a 0.2μm silicon bipolar process supplied by ST, which is characterised by three layers of metal and the cutoff frequency of the BJT above 20GHz. The overall circuit area is 1mm² (Fig. 2) for a core dimension of 0.64mm². The main core area contribution is due to the need to decouple the transformer (250μm × 250μm) and the inductance L_3 (160μm × 160μm). This distance must be at least 400μm, to obtain an acceptable magnetic decoupling between the two structures [5]. To reduce substrate coupling, thick grids of iso-

lating trenches under each inductor were designed (for the sake of clarity these structures are not shown in Fig. 2).

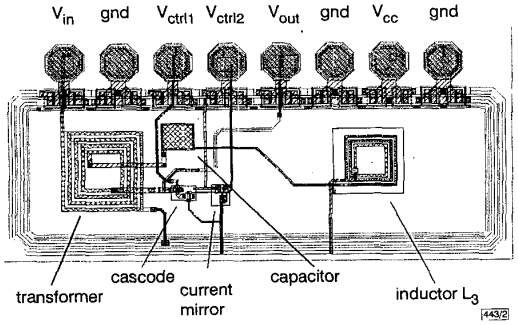

Fig. 2 *Layout of inductor*

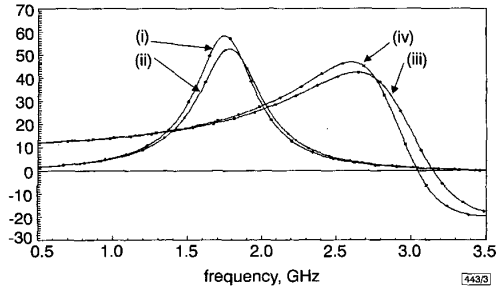

Fig. 3 *Equivalent inductance and quality factor*

(i) Q pre-layout
(ii) Q post-layout
(iii) L pre-layout
(iv) L post-layout

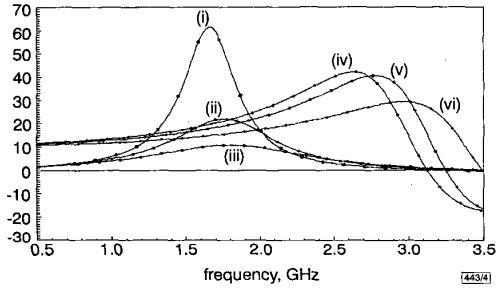

Fig. 4 *Equivalent inductance for given process and temperarure conditions*

Post-layout simulations, 1.8GHz
(i) Q = 47
(ii) Q = 20
(iii) Q = 10
(iv) L = 22nH
(v) L = 18nH
(vi) L = 16nH

Simulation results: The behavioural modelling of the transformer (inductors L_1 and L_2) and the passive inductor L_3, considered as linear two ports, was derived by using the finite difference time domain (FDTD) method [6]. The extracted Z parameters were input to the ELDO™ simulator to obtain the overall circuit electrical response. The inductance seen at the input terminals (equivalent inductance) is presented in Fig. 3 together with the quality factor. At a frequency of 1.8GHz the equivalent inductance value was 22nH, while the Q was > 45. Fig. 3 also shows the post-layout simulation result for the typical case. By properly controlling the transistor bias, the equivalent inductance could be kept within a 2% range for all process conditions and temperature ranges. A self-adaptive circuit could be also obtained by closed-loop control of the transistor bias. Finally, Fig. 4 presents, for a given process and temperature conditions (typically 27°C), how the control technique could be used to vary the equivalent inductance value from 16 to 22nH while never allowing the quality factor to fall below 10. The simulated overall power consumption was 2.6mW while the maximum current that could be driven by the active inductor was 1.5mA, which was dependent on the bias base current of Q_1.

Conclusions: In this Letter a voltage-variable, high quality active inductor designed to be realised using a standard silicon bipolar process has been presented. The inductance realised was 20nH, with a Q of 47, at 1.8GHz. The results obtained are very promising for the single-chip integration of mobile communication transceiver RF circuits.

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G. D'Angelo, A. Monorchio, A. Monterastelli and B. Neri (*Dipartimento di Ingegneria dell'Informazione, University of Pisa, Via Diotisalvi 2, I-56125 Pisa, Italy*)

L. Fanucci (*CSMDR, National Research Council, Via Diotisalvi 2, I-56126 Pisa, Italy*)

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SiGe bipolar 5.5GHz dual-modulus prescaler

B.-U. Klepser

A SiGe bipolar dual-modulus ÷64/65, ÷32/33 prescaler implemented in commercially available Infineon SiGe bipolar technology is presented. A maximum operational frequency of 5.5GHz has been measured for a supply current of 6mA at 3.3V. For a reduced supply current of 3.5mA, a maximum frequency of 4.0GHz has been obtained. A comparison with a purely-Si prescaler clearly demonstrates the enhanced speed-power product of the SiGe technology.

Introduction: Phase locked loop (PLL) synthesisers for radio frequencies from 200MHz to 5.7GHz are one of the key components of wireless communication systems. PLLs usually consist of a bipolar high-speed dual (or multi-) modulus prescaler and a programmable CMOS divider, phase detector and charge pump. For low cost mobile phone applications, both components are usually integrated on one chip using BiCMOS technology. A dual-modulus high speed prescaler is, therefore, both a stand-alone bipolar IC for a two chip 0.5–5.5GHz PLL and a building block for a one-chip SiGe BiCMOS PLL.

Silicon bipolar prescalers are mainly used for PLL synthesisers up to 3GHz [1], while for higher frequencies GaAs MESFET or HBT [2] PLLs are primarily used. With the advent of commercially available SiGe technologies with GaAs-like transit frequencies above 50GHz [3, 4], SiGe technology will increasingly be used to implement ICs for the 3.5 and 5.7GHz ISM, U-NII bands [4], and low power 900–2500MHz mobile communication BICMOS PLLs. In this Letter, a bipolar SiGe dual-modulus prescaler circuit is reported for the first time.