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Base coupled differential amplifier: a new topology for RF integrated LNA

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SUMMARY

A new topology of bipolar low noise amplifier (LNA) for RF applications, named base coupled differential (BCD), is presented. The proposed approach is compared by simulation against most classical topologies. The BCD configuration has the key advantage to join an integrated matching on a single-ended input with a differential output. This is done by using down-bond wiring, so that no integrated inductors are needed. The main advantages of this new topology are a drastic area reduction and an increased linearity range (or a reduced biasing current with the same linearity) together with a noise figure (NF) and voltage supply reduction. Particularly, the BCD LNA presented in this paper has been designed for 2.44 GHz frequency operation. It is characterized by a NF of 1.93 dB, a voltage gain (Av) of 19.5 dB, an input impedance of 50 Ω a third Input-referred Intercept Point (IIP_3) of −7.25 dBm and a dissipated power (P_D) equal to 19 mW. Copyright © 2003 John Wiley & Sons, Ltd.

KEY WORDS: low noise amplifier (LNA); bipolar technology; radio frequency

1. INTRODUCTION

The first stage of any integrated receiver for wireless applications is a low noise amplifier (LNA). The design of this stage is very difficult since it has to be compliant with several specifications. The most important are: the noise figure (NF), the input dynamic range, the matching of the input impedance to 50 Ω and the dissipated power. Moreover, a differential topology to reduce the effects of common mode interferences is recommended for LNA in wireless applications. Typically, this choice has the drawback to require a balun transformer between the antenna and the input of the amplifier and to determine an increase of the dissipated power.

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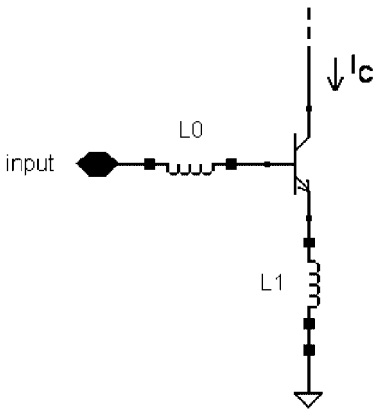

Figure 1. Input matching technique.

Another target of the LNA design is the so-called *integrated matching*, which means to simultaneously match the minimum NF and the maximum power with $Z_{in} = Z_{ON} = 50\,\Omega$, being Z_{in} the input impedance and Z_{ON} the optimum source impedance for the NF [1]. It has been demonstrated that this result can be achieved in integrated form by suitably choosing the transistor quiescent point and by using two inductors as shown in Figure 1.

By proper dimensioning L_0 and L_1 and by choosing a suitable value for the biasing current I_C and the area size of the input transistor, the integrated matching can be obtained [1,2]. It is well known that the utilization of integrated inductors causes some problems mainly due to the quite low value of their quality factor Q (typically Q is lower than 10) and to the large area occupied on die. Particularly, the low Q implies a not negligible series equivalent resistance, which impairs the NF, and the large area has a negative impact on yield and cost. For this reason, whenever it is possible, inductors are realized by exploiting wire bonding [3]. Unfortunately, this solution can be adopted only when the inductor is connected in series with an external lead or with the back grounded plane.

In the past, several LNA topologies have been proposed, but the most widely utilized are the common emitter, with an emitter degeneration, and the cascode configurations [4].

Taking into account all the above considerations, in Section 2, we propose a new topology of bipolar LNA named base coupled differential (BCD). This approach allows a reduction of the die area and an increase of the dynamic range without causing any performance degradation in terms of NF, dissipated power and gain. A comparison among the BCD topology and the most common ones has been carried out and the results of the simulations are summarized in Section 3. In Section 4 these results are discussed and finally some conclusions are drawn in Section 5.

2. BASE COUPLED DIFFERENTIAL AMPLIFIER

The proposed BCD amplifier is shown in Figure 2, where some details are omitted for sake of clarity. Particularly, I_B represents a DC current source implemented by a current mirror scheme. L_1 is realized by means of down-bonding wire to the ground plane and L_0 is obtained by using bonding wire to the input pad: both of them are necessary to obtain the

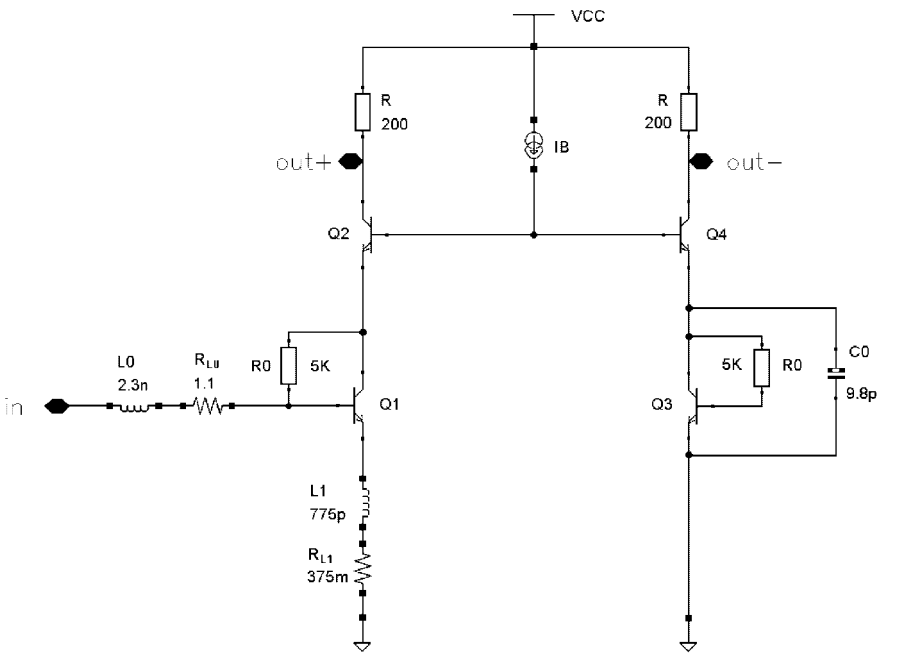

Figure 2. Base coupled differential (BCD) amplifier.

integrated input matching. The Q values for the wire bonding inductors have been estimated in 30.

If C_0 is not considered, the scheme recalls two cascode stages connected back to back each other through the bases of transistors Q_2 and Q_4. For small signals, $i_{b2} = -i_{b4}$, where i_{b2} and i_{b4} are the base current small signal variations of Q_2 and Q_4, respectively. At low frequencies, at which the effects of the intrinsic capacitances of the transistors are negligible, $i_{b2} = i_{e2}/(h_{fe2}+1)$ and $i_{b4} = i_{e4}/(h_{fe4}+1)$. Here, i_{e2} and i_{e4} are the small signal variations of the emitter current while h_{fe2} and h_{fe4} are the current gain, of Q_2 and Q_4, respectively. In the ideal case $h_{fe2} = h_{fe4}$, then the variations of the emitter currents of the two transistors and, consequently, those of the respective collector currents, have the same magnitude, but opposite sign. Therefore, a perfectly symmetric output is obtained and the amplifier realizes the aforementioned transition from a single-ended input to a differential output, in an ideal way.

This solution combines three undeniable positive aspects for LNA design: (i) maximum linear operating range according to Reference [5], also confirmed by the simulation results reported in Section 3; (ii) high common mode interference rejection due to the differential configuration scheme; (iii) reduced silicon area and noise since high quality factor ($Q > 30$) inductors, realized by means of wire bonding, are used instead of integrated inductors.

The operating point is the same for Q_2 and Q_4. The shunt capacitor C_0 has been introduced to reduce the input impedance seen from the base of Q_4. At high frequencies, its effect is very important to obtain the opposite values of Q_2 and Q_4 collector currents. SpectreRF^{TM} simulation results have shown that a slight unbalancing of the output voltages can be completely recovered by adding a very low value capacitance (tens of fF, not shown in

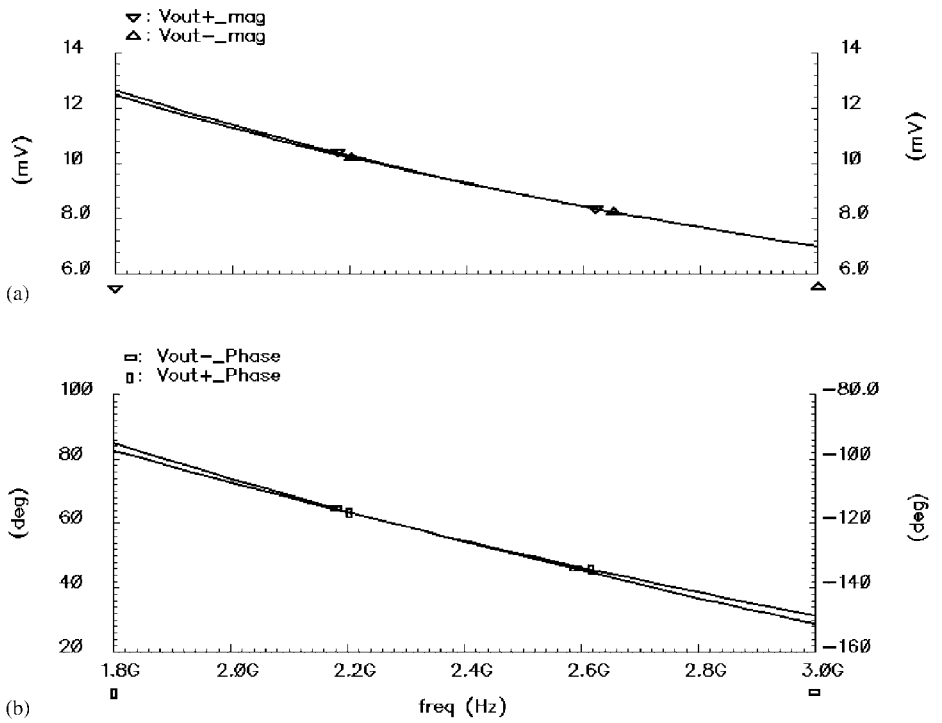

Figure 3. BCD output voltages: (a) magnitude and (b) phase.

Figure 2) between the collector and the base of Q_2. The Figure 3 shows the output voltages of the BCD stage (V_{out+} and V_{out-} signals), both in magnitude and in phase, for the frequency range of interest and for 1 mV of input signal. The symmetry of the two output with respect to ground, around 2.44 GHz, is remarkable.

3. DIFFERENT TOPOLOGIES: SIMULATION RESULTS

The comparison has been carried out among different topologies characterized by a single-ended input signal, so that no balun is required.

In that respect, one of the most widely used configurations for low cost wireless applications is the differential cascode, named emitter coupled differential (ECD), shown in Figure 4.

The inductors (L_0, L_1 and L_2) realize the integrated matching. The considered L_0 can be implemented by a bonding wire plus a microstrip while L_1 and L_2 have to be integrated on chip. The parasitic series resistance of L_0 has been calculated by considering a quality factor Q nearly equal to 30. The on-chip inductors, L_1 and L_2, have been calculated by considering $Q=8$. They are characterized by an area size of about $100\ \mu m \times 100\ \mu m$ each. The main advantage of this solution is the bandwidth and the immunity to the common mode interferences, on the contrary, the main drawback is the impossibility to exploit the down-bonding to implement L_1 and L_2 for the integrated matching. This is due to the fact that the emitters of Q_1 and Q_2 have to be connected to the internal current source. Another negative

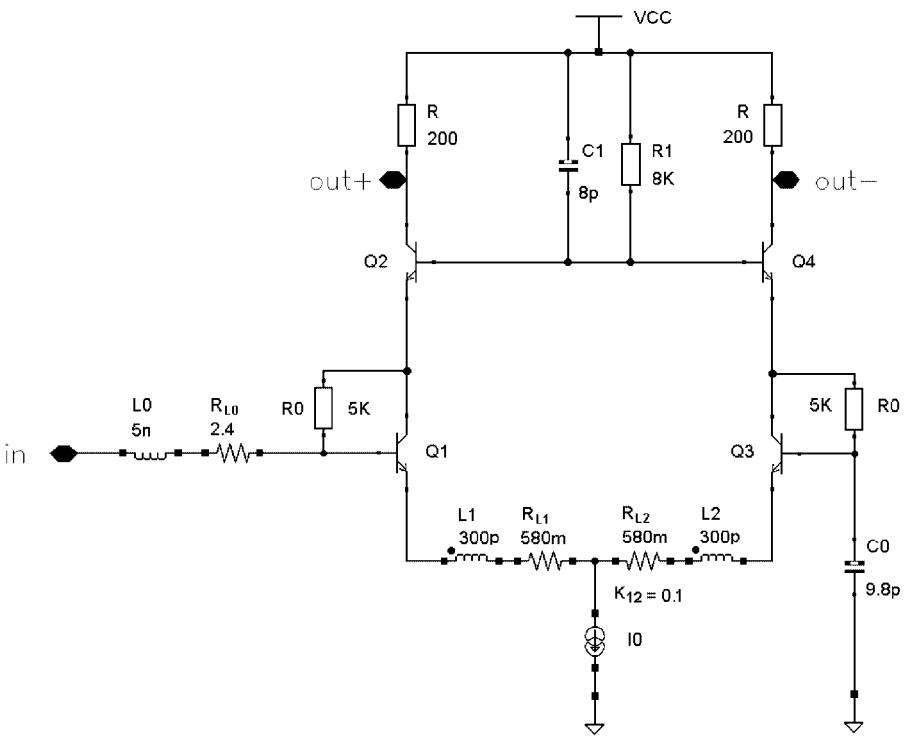

Figure 4. Emitter coupled differential (ECD) amplifier.

aspect is the reduced linearity, if compared with a single-ended cascode amplifier (as the BCD). In fact, Meyer has demonstrated in Reference [5] that, at a fixed dissipated power, the differential pair transconductance stage exhibits an IIP3 about twice lower than that of the common emitter stage.

The comparison has been also extended to the circuit configuration shown in Figure 5, named double stage differential (DSD), where the differential amplifier follows a single-ended cascode, in order to obtain a differential output. In this case, down-bonding wire can be exploited to realize the input integrated matching.

For each configuration the design has been carried out to obtain the best tradeoff between power consumption, noise figure and area size; obviously, the values of the DC current I_B and I_0 are different for each case.

As seen in Section 1, many parameters are normally used to summarize the LNA performances. For a reasonable comparative analysis among the different schemes, the choice has been done to keep constant some of them. Because the most significant parameters of a LNA are the NF and the gain at 50 Ω of source impedance, the biasing point has been chosen in such a way to obtain the same NF (which, in this case, is very close to the minimum NF of the transistors) so, in all the cases, the integrated matching has been realized. Moreover, gain and output impedance are the same for all configurations.

The amplifiers have been designed by using the HSB3 (high speed bipolar) bipolar process by ST microelectronics. It is a polysilicon self-aligned process (with three levels of metals) for

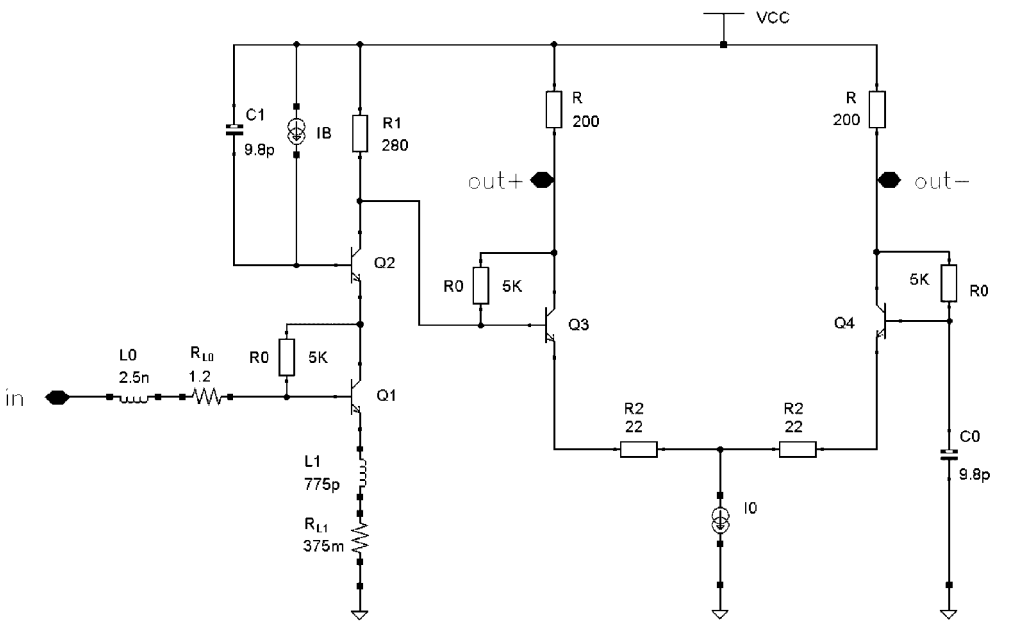

Figure 5. Double stage differential (DSD) amplifier.

Table I. Simulation results; A_v is the forward voltage gain (V_{out}/V_{in}); IS is the reverse voltage gain (V_{in}/V_{out}) evaluated at 2.54 GHz; PSRR is the ratio A_v/A_{CC}, where A_{CC} is $V_{out}/\Delta V_{CC}$ at 2.54 GHz.

	BCD	ECD	DSD
NF (dB) @ 2.44 GHz	1.93	2.50	2.23
A_v (dB) @ 2.44 GHz	19.5	19.5	19.5
Z_{in} (Ω) @ 2.44 GHz	50	50	50
P_D (mW)	19	21.3	25.8
IIP_3 (dBm)	−7.25	−8.8	−13.3
IS (dB) @ 2.54 GHz	−53.9	−54.9	−70.1
PSRR (dB) @ 2.44 GHz	21.55	10.97	19.16
Area (mm^2)	0.027	0.077	—
Down-bonding	Yes	No	yes

RF application, with 50 GHz of cut-off frequency. The transistors used have up to three base contacts in order to reduce the intrinsic resistance, and so, to offer the best noise performances. The quality factor values of the inductors taken into account here are typically obtainable at the considered operating frequency (2.44 GHz) and they have been suggested from practice.

The simulations results have been performed by means of SpectreRF™, a commercial RF analog circuit simulator integrated within the Cadence™ design framework. Periodic steady-state analysis has been utilized to predict the third intercept point (IP_3) and the 1 dB compression point ($CP_{1\,dB}$). The best results obtained for each configuration are reported in Table I and discussed in Section 4. The IIP_3 has been evaluated considering two input tones at frequencies $f_1 = 2.432$ GHz and $f_2 = 2.448$ GHz. The 1 dB input compression point

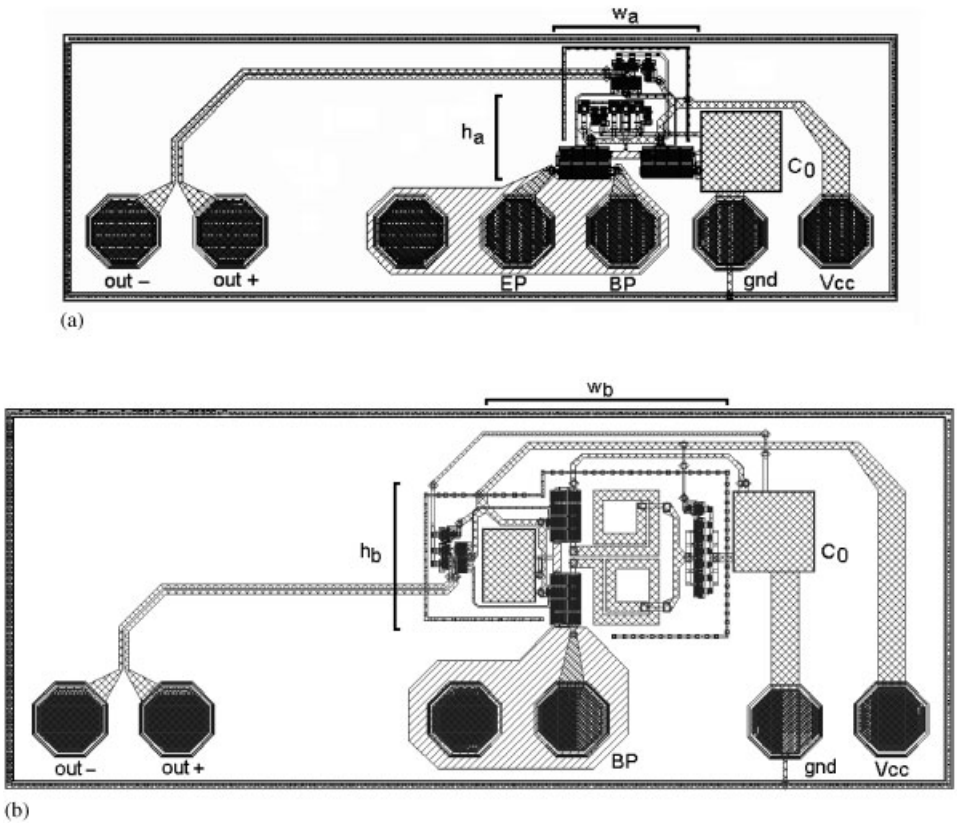

Figure 6. (a) BCD layout: total area (double trench included) $= 404 \times 1260\,\mu m^2$; $h_a = 125\,\mu m$, $w_a = 215\,\mu m$; (b) ECD layout: total area $= 574 \times 1430\,\mu m^2$; $h_b = 205\,\mu m$, $w_b = 375\,\mu m$.

($ICP_{1\,dB}$) is approximately 9.6 dB lower than IIP_3 for all the considered configurations, so that it has not been reported in Table I. The load impedance has been considered equal to 1 KHz, which is nearly the input impedance presented by the following buffer stage.

Figure 6 shows the layouts of the BCD and the ECD amplifiers (a) and (b), respectively. In both of them, BP is the ground shielded pad connected to the base of the input transistor $Q1$; in Figure 6(a) EP is the ground shielded pad connected to the emitter of the input transistor $Q1$ which has to be down-bonding wired to the back grounded plane.

Clearly, the area required by the ECD is larger mainly due to the integrated inductors. The layout of the DSD amplifier is not shown because it is characterized by the same area complexity as the BCD since it does not require any on-chip inductors.

To obtain an exact comparison in terms of area, the same distance between input and output terminals has been preserved. In the area size ($h \times w$ product) reported in Table I, the area contributions of the capacitor C_0 and of the output buffer stage have not been taken into account considering only the contribution of the amplifier itself. It is worth noting that the DC current source I_B of the BCD amplifier is generated by means of a proportional to absolute temperature (PTAT) cell which requires a larger area than a simple current mirror.

4. COMPARISONS AND DISCUSSION

The main parameters in Table I, which have been considered for the comparison, are: the dissipated power P_D, the IIP_3, the area size and the minimum value required for the power supply V_{CC}. As far as P_D is concerned, it is worth noting that, in both ECD and DSD configuration, the total current is greater that I_0. Indeed, in Figures 4 and 5 the current mirror realizing the current source is not represented. The current I_0 has been obtained by using a current mirror realized by means of two transistors whose area ratio is $\frac{1}{6}$, so that, in this way, the total current supplied by the batteries is $I_0 + I_0/6$.

Other parameters to be considered are isolation (IS) and power supply rejection ratio (PSRR). The former is defined as the ratio V_{in}/V_{out} (measured by supplying the output with a small signal and by shunting the input with a 50Ω resistor), which gives a measurement of the possible effects of the local oscillator to the input (oscillation frequency has been considered equal to 2.54 GHz). PSRR is A_v/A_{CC}, where A_{CC} is the ratio between the output voltage (V_{out}) and a possible disturb superimposed to the power supply.

The first comparison is carried out between BCD and DSD configurations since they are characterized by the same area complexity. In fact, both of them do not require any integrated inductor. The superior performances of the BCD are apparent for all the considered parameters, with the exception of the IS. The main advantage of BCD is the higher value of IIP_3, whereas the main drawback of DSD is the dissipated power which is larger by a factor of about 35%. The reduced value of IIP_3 for the DSD is due to the fact that the path between input and output is made up by a larger number of active devices (two for BCD and three for DSD). In the attempt to improve the IIP_3 for the DSD, a modified configuration has been considered where the input cascode stage is replaced by a CE stage (as shown in Figure 7): the simulation

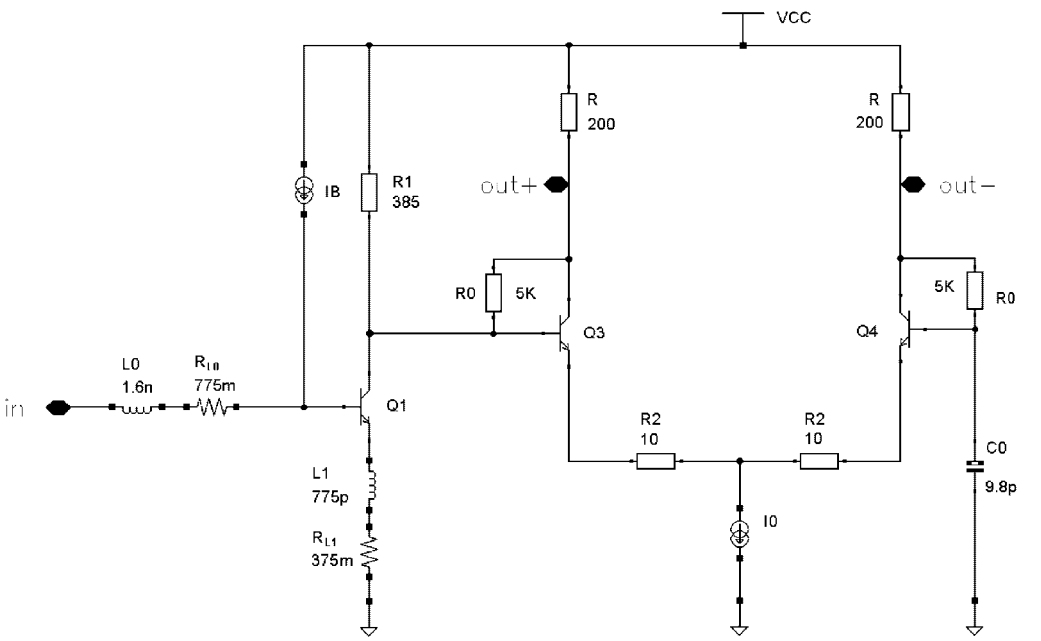

Figure 7. Double stage differential (DSD) amplifier with common emitter as first stage.

results showed a slight increase of IIP_3 at the expenses of a degradation of the isolation by a factor of about 20. For this reason this solution has not been reported in Table I.

The second comparison is carried out between BCD and ECD configurations. The superiority of the BCD is quite evident also in this case, even if the ECD performances are better than those of the DSD. Particularly, two are the main advantages of the BCD: (i) the smaller area size and (ii) the smaller input-referred third-order intermodulation distortion. The former advantage (i) does not require any further clarification: a comparison among the layouts reported in Figure 6 clearly show the negative impact on the area occupancy of the integrated inductors: the product $w \times h$ is nearly 3 times larger than the one of the BCD solution. The latter advantage (ii) derives from the single-ended input which permits to obtain a larger linearity range, according to Meyer's demonstration [5]. This is clearly validated by the data reported in Table I showing that BCD is characterized by the highest value of IIP_3.

5. CONCLUSIONS

In this paper, we have presented the BCD as bipolar amplifier topology which allows an integrated matching on a single-ended input with a differential output. No integrated inductors are needed but down-bonding wire are used to realize the emitter inductive degeneration. The symmetry of the output voltages with respect to ground has been demonstrated and it has been confirmed by simulation results. The quasi-ideal differential behaviour has been confirmed also taking into account the parasitic effects of physical layout, for the HSB3 bipolar technology by ST Microelectronics, and packaging. This scheme has been employed to realize a LNA in a 2.44 GHz RF front-end for wireless local area network (WLAN) applications. The chip has been packaged in a TQFP 48 with exposed pad.

A detailed comparative analysis with widely used traditional configurations, namely emitter coupled differential (ECD) and double stage differential (DSD), has been performed. With respect to the DSD solution, BCD shows a larger linearity range and a lower power consumption. With respect to ECD, BCD shows a higher linearity range (or a lower power consumption with the same linearity), an area complexity approximately three times smaller, a better noise figure and power supply rejection ratio.

Finally, it is worth mentioning that BCD overall performances are among the best reported in References [6–8] in the last years in bipolar technology, particularly as far as NF is concerned.

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