A High-Gain, Low-Noise, +6dBm PA in 90nm CMOS for 60-GHz Radio

M. Khanpour[+], S. P. Voinigescu[+], M. T. Yang[*]
[+]ECE Department, University of Toronto, Toronto, ON, M5S 3G4, Canada
[*]Product Engineering Special Program, TSMC, Hsin-Chu, Taiwan, ROC

***Abstract* — A 60-GHz power amplifier with 14 dB gain, 5 dB simulated noise figure, and a saturated output power of +6 dBm was fabricated in a 90nm GP process with a 9-metal digital back end. The amplifier employs two cascode stages and a common-source output stage with inductive degeneration. It has a power-added-efficiency of 6% while consuming 45 mW from a 1.5-V supply. The robustness and repeatability of the small signal and large signal performance were characterized across dies, power supply voltage, and over temperature up to 125°C. The design was also scaled to 85 GHz in 65nm CMOS with +5 dBm P_{sat}.**

***Index Terms* — 60-GHz radio, millimeter-wave amplifiers, CMOS, power amplifiers**

I. Introduction

With 3 GHz (59-62 GHz) of continuous bandwidth overlap worldwide, the 56-65 GHz frequency band offers an interesting possibility for in-room wireless distribution of uncompressed HDTV video signals at data rates exceeding 3 Gb/s. Since the first publications in 2004 reporting SiGe HBT and CMOS amplifiers [1]-[3], downconvert mixers [1], PAs [4] and directly modulated transmitters [5], the number of papers addressing 60-GHz radio ICs has sky-rocketed. One of the major benefits of implementing a gigabit-rate radio at 60 GHz is that a robust, narrow-band super-heterodyne architecture can be employed, as shown in Fig. 1. In conjunction with the smaller area of the radio front-end, and the simplified digital-signal-processing, this can lead to a lower cost radio than an alternate solution in the 2-10 GHz band. Over the last two years, it has been demonstrated that this system architecture with fundamental frequency VCO can be realized in a 160-GHz SiGe HBT technology [6],[7]. A 60-GHz receiver without VCO [8], and a 60-GHz upconverter [9] were also developed in standard 90nm GP CMOS technology. Each of these circuits, including an entire 65-GHz SiGe BiCMOS transceiver [7], occupy less than 1mm^2 of silicon.

In this paper we combine a previously reported 90nm CMOS PA with +6 dBm output power and 5 dB gain [10], with a 14-dB gain LNA [10] to create a 60-GHz CMOS power amplifier with high gain, 6% efficiency, and +6 dBm of saturated output power that also doubles up as a high linearity low-noise amplifier. Together with the double-balanced Gilbert-cell upconverter in [9], which also includes a 60-GHz LO buffer, a differential version of this PA can form the basis of a 60-GHz radio transmitter in CMOS that can deliver +9 dBm into a differential antenna load.

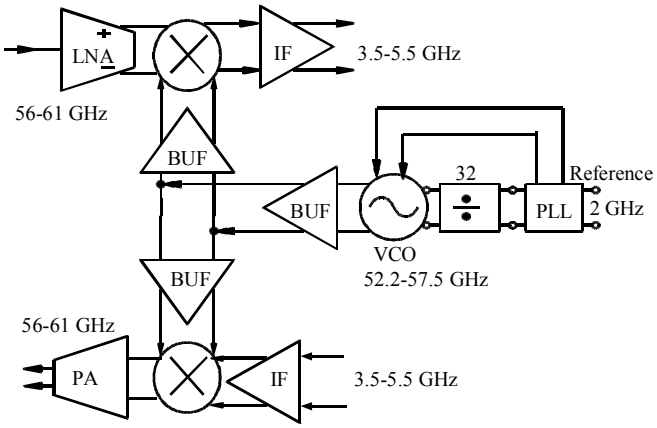

Figure 1. Superheterodyne 60-GHz radio transceiver with digital or analog IF in the 3.5-5.5 GHz range.

II. Circuit Design

A. Transistor Small Signal Model

Fig. 2 shows the simplified small signal equivalent circuit that describes a MOSFET or SiGe HBT at millimeter-waves. In addition to the gate resistance, R_g (~90Ω for a 1μm-wide finger), this representation accounts for the source degeneration resistance, R_s (200Ω×μm) and for the Miller capacitance. Both effects become stronger with technology scaling. The advantage of this equivalent circuit, where $C_{gseff} = C_{gs}/(1+g_mR_s)$, $C_{gdeff} = C_{gd}/(1+g_mR_s)$, $g_{meff} = g_m/(1+g_mR_s)$ and $g_{oeff} = g_o/(1+g_mR_s)$, is that the measured or simulated f_T and g_{meff} can be employed directly in hand analysis to accurately calculate the input and noise impedances of the transistor.

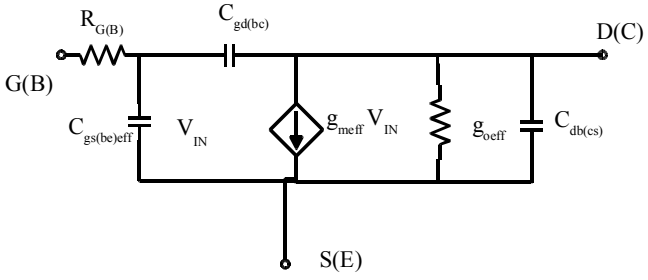

Figure 2. Simplified MOSFET or HBT equivalent circuit.

This work was funded by NSERC.

B. Topology Choice and Component Sizing

The schematic of the 3-stage power amplifier, shown in Fig. 3, indicates bias currents and component values. The amplifier consists of two cascode stages (first stage with inductive degeneration) followed by a common-source CS output buffer, also featuring inductive degeneration. The choice of a CS output was dictated by the desire to maintain good efficiency [10],[11] while the two cascode stages are employed for higher gain. The first cascode stage is biased at 0.2 mA/μm and sized according to (1) and (2) for simultaneous noise and input impedance matching, as in a low-noise amplifier.

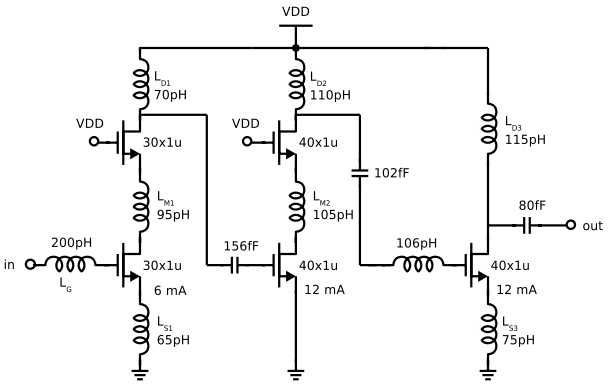

Figure 3. Amplifier schematic.

$$R_{in} = Z_0/[1+(\omega Z_0 C_{PAD})^2] = R_s+R_g + L_S\,\omega_T(casc) \qquad (1)$$

$$R_{sopt}=Z_0/[1+(\omega Z_0 C_{PAD})^2]=R_s+R_g+f_T(casc)/(2fg_{meff}) \qquad (2)$$

From (1) and (2) it becomes apparent that unlike at GHz-frequencies, where the impact of the pad capacitance is negligible, at 60 GHz the real part of the input impedance and of the optimum noise impedance of the amplifier are frequency-dependent. The pad capacitance, approximately 25fF, decreases the value of the required input and noise impedance of the amplifier to 40 Ω [12]. The role of inductors $L_{M1,2}$ is to increase gain and reduce noise figure [11].

The second and third stages are biased at 0.3 mA/μm. The third stage is inductively degenerated, for maximum linearity. The output stage is sized for a saturated output power of 6.5 dBm with 1.5 Vpp output swing. According to load-pull theory, the optimal load resistance required for maximizing the saturated output power is 62.5 Ω. This is a convenient feature of this particular design because it simplifies matching to the 50-Ω load and reduces the danger of amplifier instability due to poor small-signal S_{22}.

The hand design was verified by simulation. In the absence of a parasitic R-C extractor, all interconnect and inductors were modeled using ASITIC. This ensures that the inductance, resistance and capacitance of interconnect are adequately accounted for. Multi-metal capacitors are employed for local supply decoupling and the multi-metal dummy fill mesh was custom-designed to minimize ground resistance and inductance, and to eliminate coupling between inductors, without leaving excessive unoccupied silicon area between them.

III. Fabrication

The circuit was fabricated in TSMC's 90nm GP CMOS technology with a 9-layer Cu back-end. Unlike in a previously reported PA from our group [10] no "thick" metal option was available. The typical peak f_T and peak f_{MAX} values for interdigitated transistors with 1 μm finger width contacted on one side of the gate and biased at V_{DS}=0.7V are 120 GHz and 200 GHz, respectively. A die photograph of the power amplifier is shown in Fig. 4. The total area is 300μm×500μm, including all pads.

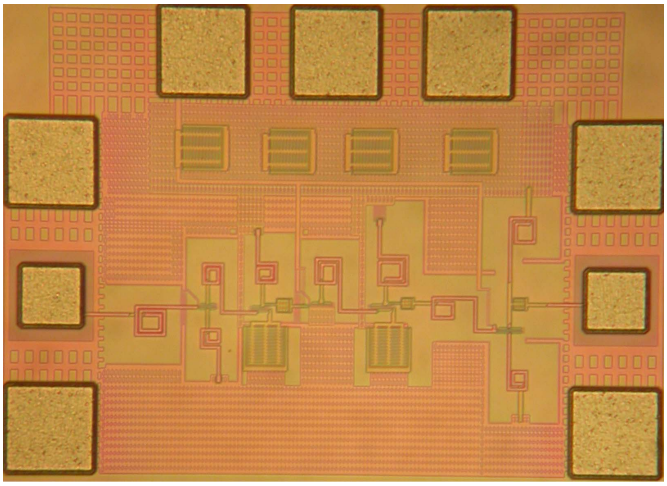

Figure 4. Die photograph.

IV. Experimental Characterization

The S-parameters were measured up to 65 GHz on 6 different dies using a Wiltron 360B VNA and 67-GHz GGB probes. These results, as well as the simulated noise figure are shown in Fig. 5, illustrating excellent repeatability with the peak gain of 14 dB centered at 55 GHz. The 3-dB bandwidth extends from 48 GHz to 61 GHz and the gain remains higher than 8 dB at 65 GHz. Both S_{11} and S_{22} are lower than -10 dB, a testament to the excellent amplifier stability, while the isolation (not shown) is better than 40 dB. The 6th die, a bit of an outlier, had an even higher gain of 15 dB. Fig. 6 shows measured S_{21} as a function of V_{DD}, illustrating that the gain drops only by 2 dB as the power supply voltage is reduced from 1.5 V to 1.2 V.

It is important to note that the input stage of the PA is identical to that of a 60-GHz LNA implemented in the same technology and whose noise figure is less than 5.2 dB at 60 GHz [11], implying that the circuit can also be employed as a low noise amplifier.

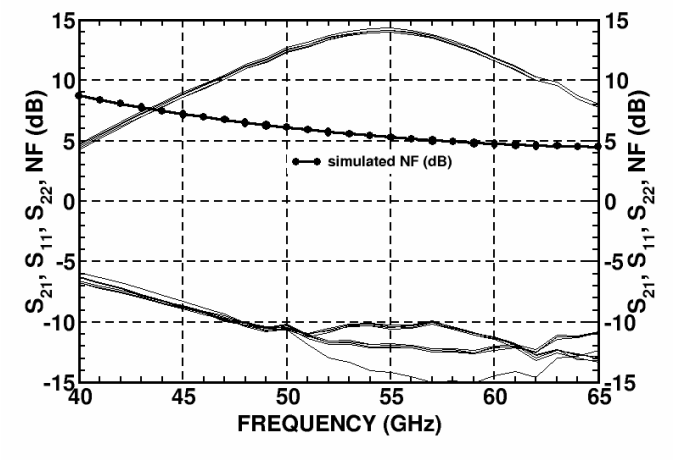

Figure 5. Measured S-parameters at room temperature across 5 dies and simulated noise figure

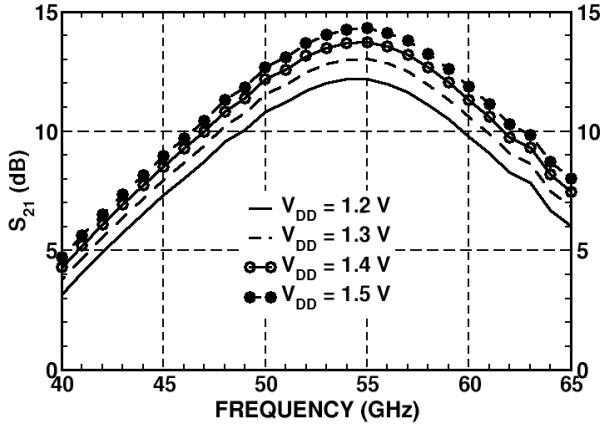

Figure 6. Measured gain as a function of frequency and V_{DD}.

Large signal measurements were conducted on a temperature-controlled probe station in the 25°C to 125°C range using an Agilent 50-75 GHz power sensor. Fig. 7 compiles the linearity and power-added-efficiency (PAE) data at 60 GHz. The maximum PAE is 6% at 55 GHz and 5.2% at 60 GHz, the saturated output power is 6 dBm while P_{1dB} is 1.6 dBm. These values result in a PA FoM=$G\times P_{sat}\times PAE\times f^2$ of 12 [$W\times GHz^2$], the highest for any 60-GHz CMOS PA reported to date [11], [12]. The saturated output power and P_{1dB} were also measured as a function of the bias current density of the transistor in the output stage. The results are compiled in Fig. 8 and confirm that the optimal linearity bias coincides with the peak f_T current density of 0.3-0.35 mA/μm [11]. However, higher bias current density of 0.45 mA/μm is needed to maximize the saturated output power. The relatively large difference of 4 dBm between P_{1dB} and P_{sat} is likely due to the linearity being limited by the smaller V_{DS} of the common-gate transistor in the second cascode stage.

Finally, the power gain, P_{sat} and P_{1dB} variation in the 25°C to 125°C temperature range are reproduced in Figs. 9 and 10, respectively. It is for the first time that such measurements have been conducted on mm-wave CMOS PA. The power gain

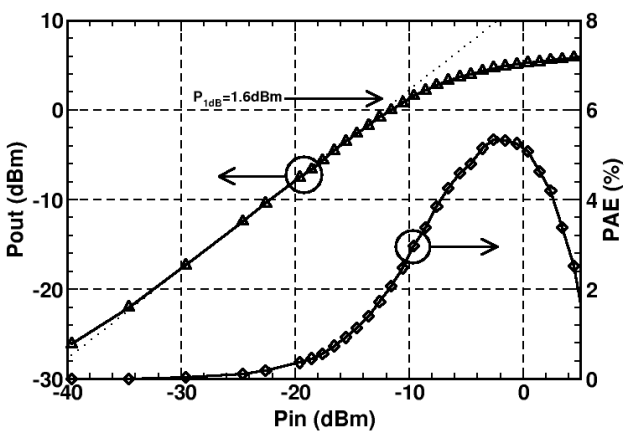

Figure 7. Measured linearity, P_{sat} and PAE at 60 GHz.

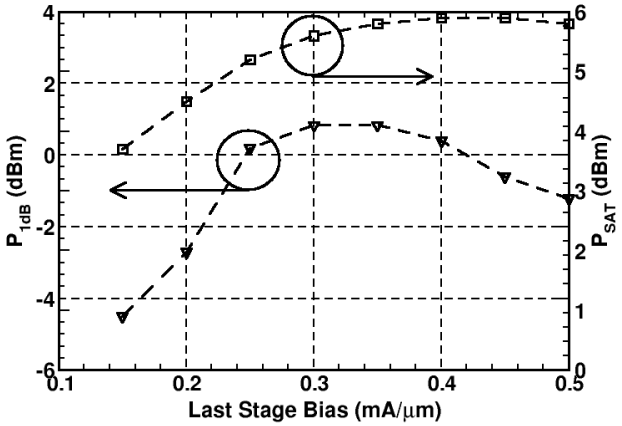

Figure 8. Measured P_{1dB} and P_{sat} at 60 GHz as a function of the drain current density of the output stage.

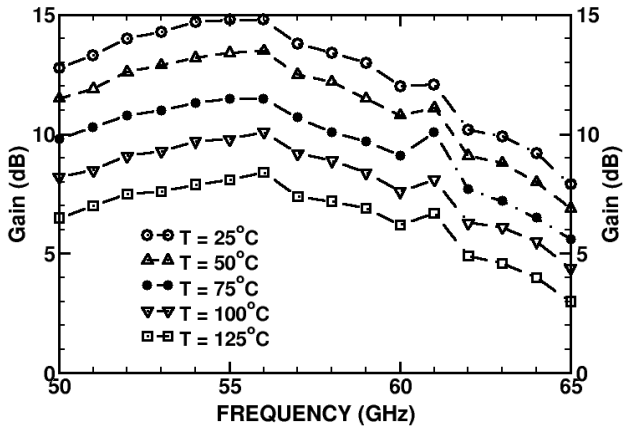

Figure 9. Measured gain as a function of frequency and temperature.

decreases by 6 dB, while the saturated output power drops by only 2 dBm from 25°C to 100°C, indicating that CMOS technology could be deployed in practical in-door radio systems at 60 GHz.

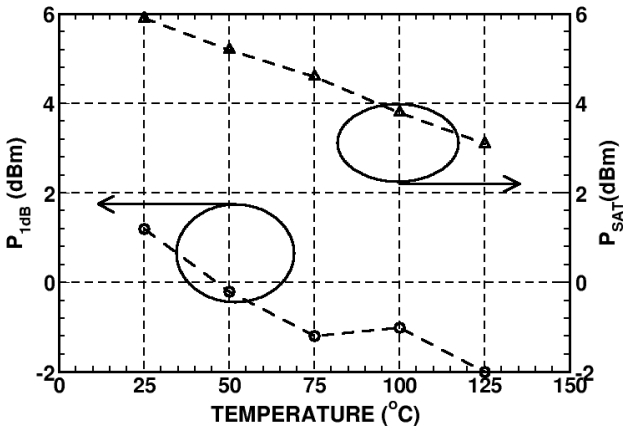

Figure 10. Measured P_{sat} and P_{1dB} at 55 GHz as a function of temperature.

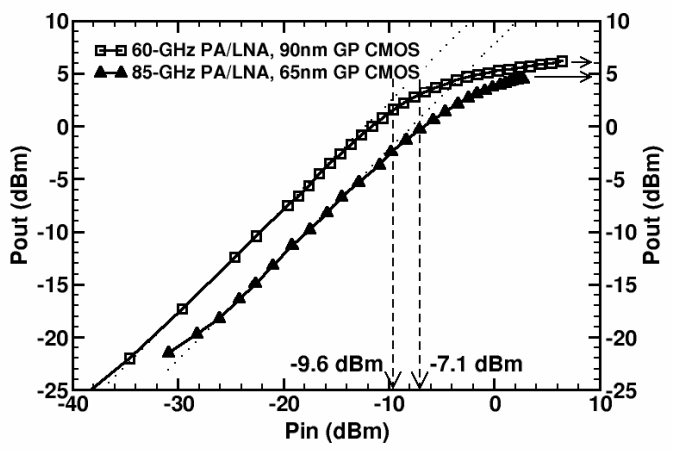

Figure 11. Linearity plots of the 60-GHz and 85-GHz amplifiers.

V. Scaling to 85 GHz in 65nm CMOS

The LNA/PA concept was recently implemented in 65nm GP CMOS at 85 GHz. A 3-stage cascode topology was employed [13] and the transistors in the output stage are identical in size (40 μm) to those in the 60-GHz LNA/PA. Fig. 11 compares the linearity curves for the two amplifiers, demonstrating that 65nm CMOS technology is capable of delivering +5 dBm of output power at 85 GHz.

VI. Conclusion

A 60-GHz power amplifier with 14 dB gain and record FoM for CMOS PAs was implemented in 90nm CMOS technology. The amplifier was characterized over process, supply voltage and temperature variation, showing excellent yield and repeatability. The performance over temperature is acceptable only up to 75°C ambient, with the power gain remaining above 10 dB. Despite this progress, the output power and the temperature behaviour of CMOS PAs remain inferior to those of mm-wave SiGe HBT PAs [14],[15], which readily deliver 16-20 dBm of output power with high efficiency and without requiring power combining techniques.

Acknowledgment

We would like to thank Jaro Pristupa and CMC for CAD tools and support. Equipment grants by OIT and CFI are also gratefully acknowledged.

References

[1] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe Bipolar Transceiver Circuits Operating at 60GHz," IEEE J. Solid-State Circuits, vol. 40,, pp. 156-157, Jan. 2005.

[2] C.H. Doan, S. Emami, A.M. Niknejad, and R.W. Brodersen, "Design of CMOS for 60GHz Applications" IEEE ISSCC Digest, pp.440-441, Feb. 2004.

[3] M. Gordon and S. P. Voinigescu, "An Inductor-based 52-GHz, 0.18μm SiGe BiCMOS Cascode LNA with 22dB Gain," in Proc. ESSCIRC, pp. 287-291, Sept. 2004.

[4] U.R. Pfeiffer, S.K. Reynolds, and B.A. Floyd, "A 77 GHz SiGe Power Amplifier for Potential Applications in Automotive Radar Systems," in IEEE RFIC Symp. Dig, pp. 91-94, June 2004.

[5] C. Lee, T. Yao, A. Mangan, K. Yau, M.A. Copeland, and S.P. Voinigescu, "SiGe BiCMOS 65-GHz BPSK Transmitter and 30 to 122 GHz LC-Varactor VCOs with up to 21% Tuning Range," IEEE CSICS, Digest, pp.179-182, Oct. 2004.

[6] M.Q. Gordon, T. Yao and S.P. Voinigescu,"65-GHz Receiver in SiGe BiCMOS using Monolithic Inductors and Transformers," in IEEE SiRF, Tech. Dig., pp. 265-268, Jan. 2006.

[7] T. Yao, L. Tchoketch-Kebir, O. Yuryevich, M.Q. Gordon, and S.P. Voinigescu, "65GHz Doppler Radar Transceiver with On-Chip Antenna in 0.18μm SiGe BiCMOS," IEEE IMS Digest, pp.1493-1496, June 2006.

[8] D. Alldred, B. Cousins and S.P. Voinigescu, "A 1.2V, 60GHz Radio Receiver with On-Chip Transformers and Inductors in 90nm CMOS," in Proc. IEEE CSICS, pp. 51-54, Nov. 2006.

[9] S.P. Voinigescu, et al., "CMOS SOCs at 100 GHz: System Architectures, Device Characterization, and IC Design Examples." in IEEE ISCAS, pp.1971-1974, May 2007.

[10] T. Yao, M. Gordon, K.H.K. Yau, M.T. Yang, and S.P. Voinigescu, "60-GHz PA and LNA in 90-nm RF-CMOS," IEEE RFIC Symposium Digest, pp. 147-150, June 2006.

[11] T. Yao, et al., "Algoriyhmic Design of CMOS LNAs and PAs for 60-GHz Radio," IEEE J. Solid-State Circuits,Vol.42, No.5, pp. 1044-1057, May 2007.

[12] S.T. Nicolson and S.P. Voinigescu, "Methodology for Simultaneous Noise and Impedance Matching in W-Band LNAs," in Proc. IEEE CSICS, pp. 279-282, Nov. 2006.

[13] K. W. Tang, M. Khanpour, P. Garcia, C. Garnier, S. P. Voinigescu, "65-nm CMOS, W-Band Receivers for Imaging Applications," CICC-2007, accepted for oral presentation.

[14] S.T. Nicolson, K.K.W. Tang, K.H.K. Yau, P. Chevalier, B. Sautreuil and S.P. Voinigescu, "A 2.5V 77GHz Automotive Radar Chipset," IEEE Int. Microwave Symp. Digest, pp.487-490, Honolulu, HI, Jun. 2007.

[15] U. Pfeiffer, "A 20dBm Fully-Integrated 60GHz SiGe Power Amplifier with Automatic Level Control," in Proc. ESSCIRC, pp. 356-359, Sept. 2006