A 20 dBm Fully-Integrated 60 GHz SiGe Power Amplifier With Automatic Level Control

Ullrich R. Pfeiffer, *Senior Member, IEEE*, and David Goren, *Member, IEEE*

***Abstract*—A +20 dBm power amplifier (PA) for applications in the 60 GHz industrial scientific medical (ISM) band is presented. The PA is fabricated in a 0.13-μm SiGe BiCMOS process technology and features a fully-integrated on-chip RMS power detector for automatic level control (ALC), build-in self test and voltage standing wave ratio (VSWR) protection. The single-stage push-pull amplifier uses center-tapped microstrips for a highly efficient and compact layout with a core area of 0.075 mm^2. The PA can deliver up to 20 dBm, which to date, is the highest reported output power at mm-wave frequencies in silicon without the need for power combining. At 60 GHz it achieves a peak power gain of 18 dB, a 1-dB compression (P1dB) of 13.1 dBm, and a peak power-added efficiency (PAE) of 12.7%. The amplifier is programmable through a three-wire serial digital interface enabeling an adaptive bias control from a 4-V supply.**

***Index Terms*—Automatic level control, bipolar transistor, built-in self-test, closed-loop power control, mm-wave, power amplifier, power detector, RMS power detector, silicon germanium, 60 GHz.**

I. Introduction

POWER amplifiers in a silicon germanium (SiGe) process technology are one of the key building blocks that enable single-chip integrated transceivers at millimeter-wave (mm-wave) frequencies. The continued device scaling [1], [2] of SiGe heterojunction bipolar transistors (HBTs) has achieved cut-off frequencies as high as $f_{\max}/f_T = 350/300$ GHz [3] which makes SiGe an ideal technology for applications like high-speed communications systems at 60 GHz [4]–[7] or automotive radar systems at 77 GHz [8].

Conceptually, single-chip integrated transceivers at mm-wave frequencies ought to be no different than their lower frequency counter parts at the cellular bands. However, the high performance SiGe HBT breakdown voltages $\mathrm{BV_{CEO}}$ and $\mathrm{BV_{CBO}}$ are typically below 2 V and 6 V respectively, which makes high-power amplifiers a challenging building block [9]. Moreover, high power gain at mm-wave frequencies is typically achieved at bias current densities close to peak $f_{\max}$. On-chip power detection circuits are therefore needed at mm-wave frequencies to implement a dynamic bias control and to mitigate the impact of process, voltage and temperature variations (PVT-variations). The harsh environmental conditions of packaged radio communication systems make voltage standing wave ratio (VSWR) protection circuits necessary to cope with varying antenna load impedances. An analog built-in self-test (BIST) mechanism is needed to facilitate low-cost and high-volume self tests.

While peak and root-mean-square (RMS) power detector circuits are routinely integrated on-chip at lower frequencies [10]–[14], they have just recently been targeted at mm-waves. For instance in [15], an on-chip power detector circuit was implemented at 24 GHz, however, the power coupler was added externally. Another example is a 20 GHz peak/RMS power detector with a wide dynamic range, presented in [16]. Advances have been made on the amplifiers with single device output powers as high as 15.5 dBm at 60 GHz [5], [9], [17]–[19] and at 77 GHz [20], [21]. On-chip power combining and balanced device operation has been exploited to enhance the maximum available output power per chip, e.g., 18.5 dBm [21], 17.5 dBm [22], and 21 dBm [23], while the PAE typically is around 10% or below.

Early results of this power amplifier have been previously published in [24]. This paper presents extended material with a detailed description of the RMS power detection principle. This includes the power coupling mechanism, the physical structure of the power coupler, and its equivalent circuit modeling. The amplifier's performance variation from 5–85 °C is included to show the need for an automatic level control to mitigate PVT-variations. The correlation of the detector output with a varying external load impedance is analyzed. Other detector usage models like build-in self tests and VSWR protection methods are supported. The performance of the input/output contact pads is presented as well as the small-signal S-parameters of the amplifier.

At 60 GHz the differential amplifier achieves a peak power gain of 18 dB with a 13.1 dBm output referred 1-dB compression point, a 12.7% peak PAE, and a saturated output power of 20 dBm. The amplifier uses center-tapped microstrips with AC grounds for a highly efficient and compact layout with a core area of 0.075 mm^2. The highest peak PAE (13%) was measured at 59 GHz. The amplifier achieves a high level of integration including an adaptive bias control that is programmable through a three-wire serial digital interface. The chip can be fully molded in a low-cost plastic packaging technology enabeling highly integrated single-chip transceivers at mm-wave frequencies as described in [6].

II. Circuit Architecture

The power amplifier was designed in IBM's advanced bipolar technology SiGe8HP. It is a 0.13-μm SiGe technology with cutoff frequencies $f_{\max}/f_T = 240/200$ GHz. The five-layer

Manuscript received November 17, 2006; revised February 23, 2007. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under Grant N66001-02-C-8014 and N66001-05-C-8013.

U. R. Pfeiffer is with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: ullrich@ieee.org)

D. Goren is with the IBM Haifa Research Laboratories, Mount Carmel, Haifa 31905, Israel, and also with the Technion–Israel Institute of Technology, Technion City, Haifa 32000, Israel (e-mail: davidg@il.ibm.com).

Digital Object Identifier 10.1109/JSSC.2007.899116

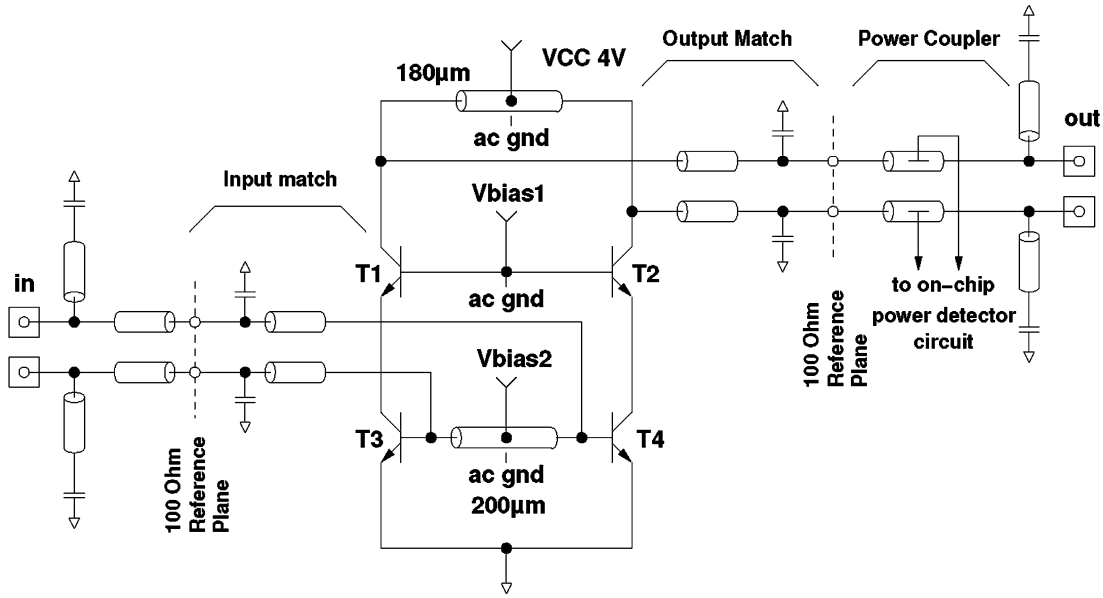

Fig. 1. Simplified amplifier schematic. The bias circuits, voltage regulators, serial interface, and power detector circuit have been omitted for clarity. Two cascode amplifiers are used in push-pull configuration with 180 and 200 μm long center-tap DC feed-lines.

back-end of the line has three copper layers with two thick aluminum layers for low loss interconnects available. The design kit includes interconnect models for side-shielded microstrips up to 110 GHz. Such models are scalable by length and width for simple circuit schematic integration. The SiGe HBT breakdown voltages are $\mathrm{BV_{CEO}} \approx 1.7$ V and $\mathrm{BV_{CBO}} \approx 5.5$ V respectively. For more information on the parasitic modeling and design approach for SiGe HBTs power amplifiers operating at mm-wave frequencies see [9].

The amplifier was optimized for good linearity, high output power, high efficiency, and high power gain. It uses a single-stage push-pull amplifier topology with two cascode gain stages. See Fig. 1 for a simplified amplifier schematic. The differential push-pull operation has two advantages: 1) it enhances the achievable efficiency of the output impedance transformation through a lower impedance transformation ratio, and 2), the power from two amplifiers is easily combined at the antenna leading to an extra 3-dB power pick-up. For instance, folded dipole antennas have a characteristic impedance of $Z_0 = 280\ \Omega$ in free space. To deliver a 100 mW (+20 dBm) into a 280 Ω differential dipole antenna with a ± 2 V collector swing, an impedance transformation ratio $R_{\mathrm{load}}/R_{\mathrm{in}}$ of 1:14 is required. This changes to 1:3.5 in case of a differential amplifier which can swing twice as high (up to ± 4 V) across two devices. This improves the efficiency of any output matching network which is an inherent advantage compared to single-ended output stages. See Section II-C for the chip-packaging concept including differential integrated antennas.

The cascode topology was preferred over a common-emitter stage for two reasons: 1) it can provide higher gain which helps the PAE, and 2), the common-base (CB) output devices (T1 and T2) can be AC-grounded at the base to provide low external base resistance. The low external base resistance minimizes impact ionization and thus maximizes the breakdown voltage of the output device. At 60 GHz, however, it is difficult to provide a good AC-ground at the CB base because of the many bypass capacitors needed to handle the large base-current swing. Such capacitors are likely to be beyond self-resonance and their residual inductance can cause stability problems which need to be avoided. To overcome this, the two cascode stages are laid out in close proximity to one another to wire their CB bases directly together. This provides an AC-ground at the base of the common-base (CB) output devices (T1 and T2) and relaxes the need for bypass capacitors in this region substantially. To the first order, the base current circulates back and forth between the two devices and only some bypass capacitance is needed to account for base current asymmetries. This allows the output voltage to swing ± 2.5 V around the 4-V DC supply voltage without causing the device to break down.

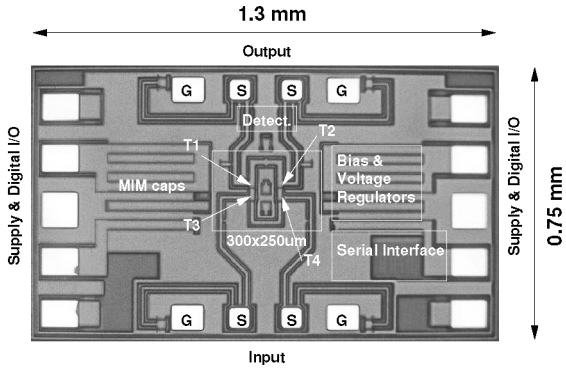

Fig. 2. Chip micrograph: The pad-limited chip has a size of 0.75×1.3 mm^2. The PA core area is only $300 \times 250\ \mu$m^2 including input and output impedance match to a 100-Ω differential impedance (each pad and shunt stub provide a 50 Ω impedance).

Fig. 2 shows a chip micrograph of the PA. The input and output pads use a ground-signal-signal-ground (GSSG) configuration instead of a conventional GSGSG case. Such a smaller spatial separation between the two signal pads provides a better

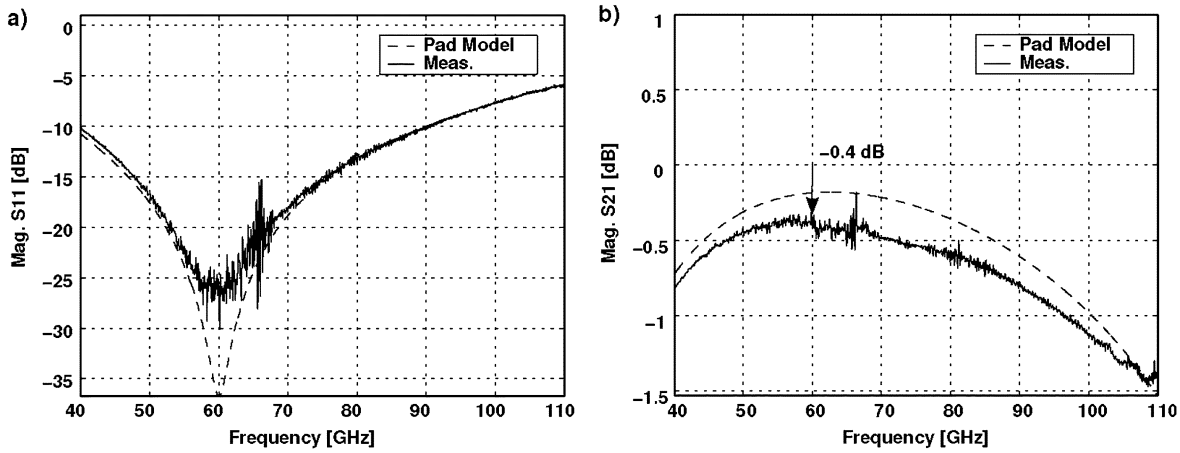

Fig. 3. Model-to-hardware correlation of the shielded contact pads. A shielded pad uses a shunt stub to resonate the pads parasitic capacitance. At 60 GHz the pad has only 0.4 dB insertion (b) with 25 dB return-loss (a) and therefore is nearly electrically *transparent* to the off-chip load impedance.

excitation of differential antenna port connection. The pad-limited chip has a size of 1.3×0.75 mm^2 including bond pads. All DC supply and control pins on the chip have electrostatic discharge (ESD) protection circuits. The PA outputs rely on the on-chip RF-choke to provide a shunt path for an ESD strike. Additional ESD protection can be added to the input and out pads where the additional ESD capacitance can be absorbed by the pads tuning stub (not currently implemented).

Another design approach was to shrink the layout as much as possible to minimize resistive losses in on-chip interconnects and matching elements. The length of typical quarter-wave RF-chokes was reduced to a twelfth of the wavelength (180 and 200 μm instead of 600 μm). In fact, the chokes use only one T-line that connects across T1 and T2. A single center-tap connection in the middle of the line is used to feed the bias supply current to both devices. The symmetric layout and push-pull operation of the PA provides an AC-ground at the center-tap connection, which relaxes the supply bypass significantly. The shorter chokes have less DC-resistance and improve the PAE.

Note, this amplifier topology is neither balanced nor truly differential. Balanced amplifiers are laid out in parallel and can not provide such AC-grounds, whereas truly differential amplifiers utilize current sources to provide circulating currents even if they are driven single ended. As a result the amplifier requires a differential drive with good phase match for optimum operation.

A. Low-Loss Contact Pad

The physical design of RF contact pads has a large effect on the power amplifier's performance and output impedance matching technique. At mm-wave frequencies contact pads are electrically large and their parasitic capacitance and losses are significant. Common practice is to simply scale the contact area down to reduce the parasitic capacitance and to limit the amount of lossy eddy currents in the substrate. There are scaling limits, however, since the minimum pad size is restricted by wire or flip-chip bonding constraints. Additional DT (deep-trench) isolation or NS (npn sub-collector) shields are commonly used to reduce losses without increasing the pads parasitic capacitance unnecessarily. Metal shields directly below the pad structure, however, have not been widely adopted due to their high capacitance.

In this work a solid metal ground shield was used right below the contact pad. The low loss weighs out the increase in capacitance since the increased pad capacitance can be tuned out by a shunt transmission line stub (see Fig. 1) that adds little loss to the structure. Larger pad structures are possible with sufficient contact area (70×70 μm^2) to comply with packaging constraints. The shunt transmission line is AC coupled to ground with a series MIM capacitor. The resonant structure is wideband and has low insertion and return-loss. It is therefore nearly electrically transparent to the off-chip load impedance. Note, the pad is not part of the impedance transformation network and the length of the on-chip transmission line that connects to the pads can have an arbitrary length while only affecting the loss but not the output match of the PA — a very convenient layout feature to accommodate various chip layouts.

The solid metal shield below the pad forms a parallel-plate capacitor which can be modeled very accurately. An equivalent lumped circuit model for the contact pad was combined with distributed transmission line models, metal-insulator-metal (MIM) capacitor models, and parasitic via inductances. The contact pad has 26 fF with a series resistance of 300 mΩ. Good model-to-hardware correlation was achieved (see Fig. 3). Around 60 GHz the pad including a 75-μm long T-line has only 0.4 dB insertion-loss, see Fig. 3(b). The measured return-loss is 25 dB, see Fig. 3(a). The measured two-port S-parameter data was derived from the error boxes of a second-tier on-chip calibration, done with a symmetric, back-to-back mounted, through pad structure. For more information on the measurement technique see [25].

B. Measured Results

Swept power gain compression measurements at 60 GHz require accurate calibration and de-embedding techniques at each power level and frequency in order to remove non-linear effects of the test equipment and any driver amplifier that may precede the device under test. To enhance the dynamic range of the measurement, a calibrated thermal power detector was used to calibrate a spectrum analyzer that uses an external harmonic mixer for measurements in the 58 to 65 GHz frequency range. The frequency dependent loss (mag S21 in dB) from the

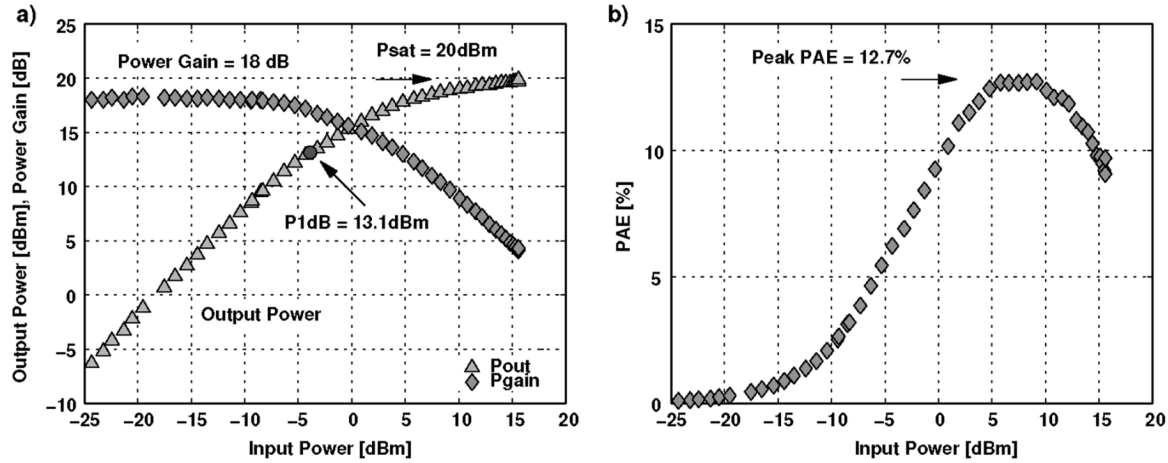

Fig. 4. Measured large-signal characteristic at 60 GHz. Power gain and output power versus input power is shown in (a), power-added efficiency (PAE) in (b).

spectrum analyzer to the output probe tip (probe included) was calibrated using a second-tier short-open-load (SOL) adapter removal technique with an accuracy of ± 0.2 dB. Note, any error in the output calibration will affect the measured output power and hence the measured PAE. The available input power from the source has been calibrated with a through measurement on a low-loss differential GSSG calibration substrate. All measurements in this paper have been made on-wafer. A pure-mode network analyzer concept described in [26] with external wave-guide balun was used to ensure phase and amplitude balanced input signals for differential measurements. This is crucial for the measurements since the amplifier requires AC-grounds for optimum performance. Single-ended data should only be measured at the output while the amplifier is driven differentially. The overall calibration accuracy of this setup is estimated to be within ± 0.5 dB for both input and output power levels.

Fig. 4 shows the measured large-signal compression characteristic of the amplifier at 60 GHz. Fig. 4(a) shows the power gain and output power versus input power. Fig. 4(b) shows a 12.7% PAE and the peak drain efficiency η is 15% at saturation. The amplifier's DC current from a 4 V supply increases from 60 mA to 160 mA at saturation. The single stage amplifier has high power gain of 18 dB at 62 GHz and the output power at a 1-dB compression (P1dB) is 13.5 dBm. The saturated output power $(P_{\rm sat})$ is 20 dBm with a 4.5-dB compressed gain.

A summary of the large-signal frequency response from 58–65 GHz in 500 MHz steps is shown in Fig. 5. Note, all large-signal measurements use an external wave-guide balun to drive the PA differentially. However, the baluns phase-shift across frequency is not constant and changes within 10° [26]. This affects the measured amplifier gain slightly as can be seen in the figure. The measured gain changes within 3 dB from 58 to 65 GHz. The saturated output power drops about 3 dB from 20 dBm to 17 dBm at 65 GHz. The P1 dB changes about 4 dB from 14 dBm to 10 dBm and the highest peak PAE is 13% at 59 GHz, which drops to 7% at 65 GHz.

Fig. 6 shows a comparison of measured small-signal S-parameters with simulation results. The return-loss in Fig. 6(b) is better than 10 dB from 59–65 GHz and agrees well with simulations. The small-signal gain in Fig. 6(b) is about 17 dB,

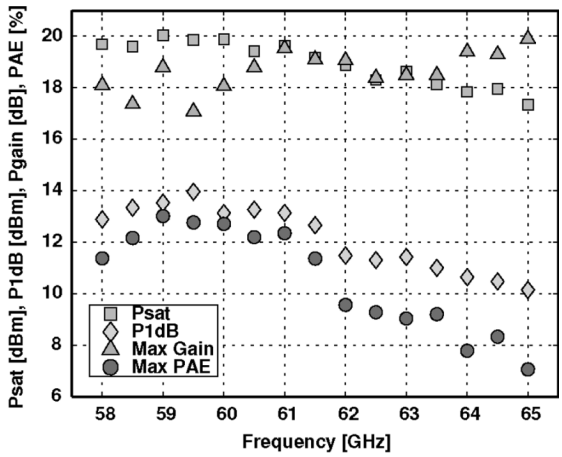

Fig. 5. Large-signal frequency response from 58–65 GHz in 500 MHz steps. The figure shows the saturated output power $P_{\rm sat}$, the output referred 1-dB compression point (P1dB), the maximum power gain and the peak power-added efficiency (PAE).

with a return isolation of -30 dB. Note, the 10° phase accuracy of the external wave-guide balun is not good enough to provide accurate back-to-back calibrations for two wave-guide baluns. Better results have been achieved with single-ended measurements where one input of the PA was terminated with 50 Ω. As mentioned before the PA is not a truly differential circuit and thus under single-ended operation will not have good AC-grounds. This affects the small-signal gain flatness shown in Fig. 6(b). The output return loss is -9 dB to -2 dB. According to Edward's stability factor ($\mu > 1$ and $\mathrm{B1f} > 0$), the circuit is unconditionally stable.

C. Chip Packaging

The PA was designed for applications in the 59–64 GHz ISM band. The PA can be packaged in a high-volume and low-cost plastic molding process together with 7-dBi cavity-backed folded-dipole antennas as has been shown in [6]. Note, in a silicon process technology, the surface of the chip is passivated and the fields of on-chip T-lines are well confined within the back-end-of-the-line (BEOL) of the technology. The electrical

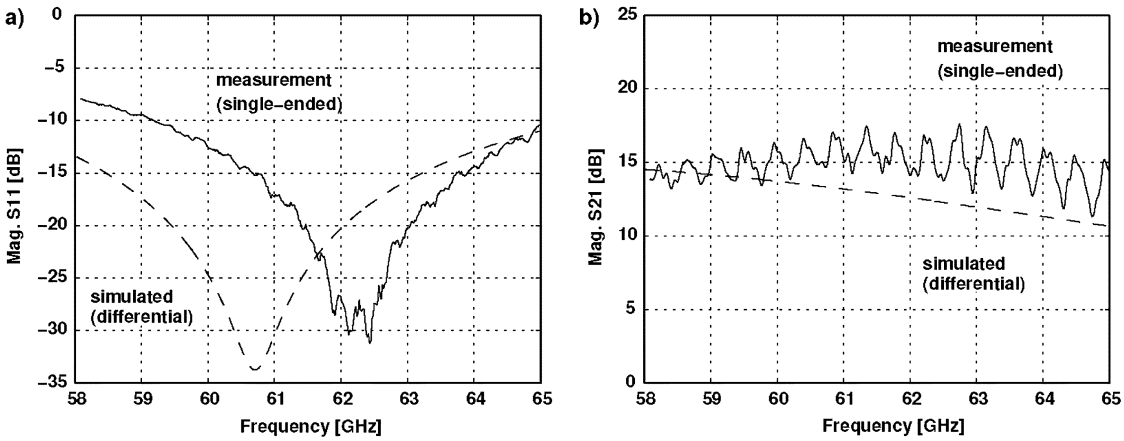

Fig. 6. Measured (solid line) and simulated (dashed line) S-parameters. Note, good S-parameter calibrations require a single-ended measurement, however, the PA is a differential circuit that will not have good AC-grounds if driven in single-ended mode. (a) shows good return-loss correlation and (b) shows inevitable gain-ripples due to the single-ended measurement.

properties of the mold material therefore are negligible during the design phase. The mold however affects the antenna which is directly flip-chip mounted to the PA. The antenna provides a 100-Ω load-line impedance rather than a conjugated match at the output to extract the maximum power from the HBTs. The PA therefore represents a mismatched reverse termination. This mismatch does not cause any voltage standing wave ratio (VSWR) problems as long as the PA is connected to a 100-Ω differential antenna and interconnect system. Power will only be reflected in a case where the antenna port impedance is mis-tuned. Under ideal environment conditions the antenna is well matched with a return-loss better than -20 dB across the 60 GHz ISM band as shown in anechoic chamber measurements in [27]. In close proximity to reflective objects this may change, but VSWR tests have indicated that detuning the antenna does not harm the output HBTs even at saturation, and stable operation is ensured under varying load conditions. Additional VSWR protection can be implemented using the on-chip power detection circuit described in the following section. If a programmable peak power level is exceeded the amplifier can be powered down within 1 μs to prevent an output devices breakdown.

III. mm-Wave Power Detector

On-chip power detection circuits are desired at mm-wave frequencies because of three reasons: 1) a dynamic bias control is needed to mitigate the impact of process, voltage and temperature variations (PVT-variations), 2) a built-in self-test (BIST) mechanism is needed to facilitate a low-cost and high-volume self test, and 3) VSWR protection is often required to enhance the device lifetime and to provide an emergency shutdown in case the amplifier is overloaded.

A dynamic bias or automated level control is routinely used in a variety of communication and measurement systems. In wireless systems, for example, the magnitude of the transmit power is controlled to improve efficiency, linearity or to ensure the transmit power is within specification as desired by various standards. Furthermore, transistors in mm-wave amplifiers are often biased at a current density close to their peak $f_{\max}$ to provide a high power gain. This makes it difficult to implement simple bias circuits to provide constant output power over PVT-variations.

A BIST mechanism is widely used in industry to verify the internal functionality of integrated circuits. The main purpose of a BIST is to reduce the cost and complexity of external test equipment. The test-cycle duration and the complexity of automated test equipment is particularly high at mm-wave frequencies. In fact, chipsets with package-integrated antennas, as described in Section II-C, do not have RF-port connectors available and require calibrated anechoic chambers for accurate radiated power measurements.

Power amplifiers in radio communication systems are likely to experience a variety of antenna load impedances which may causes standing waves at the output. An adaptive bias scheme or an emergency shutdown in therefore required for protection and a VSWR protection method is needed to keep the amplifier well outside the transistors breakdown region.

A RMS power detection is more useful than peak power detection because it can measure a modulated signal independent of its waveform shape. There are several types of root mean square (RMS) power detectors mentioned in the literature [16]. They can be divided into thermal detectors or square-law detectors. Thermal detectors, e.g., bolometers, measure the temperature change in a resistive component with respect to the ambient temperature [28], [29]. The temperature difference is proportional to the applied RF power. Square-law detectors use either diodes, e.g., Schottky diodes or npn/FET transistors, to convert a voltage amplitude into a signal proportional to the RF power [28]. The detector output is typically low-pass filtered to provide an adequate DC output level.

The on-chip power detector in this paper uses a power coupler, see Section III-A, and a power detection circuit as shown in Fig. 7. The power coupler uses tiny capacitors that are integrated inside the amplifier's output transmission lines (T-lines). The physical structure of the T-line has been altered only locally to absorb the coupling capacitor into the distributed elements of the line. The couplers therefore do not change the characteristic impedance or the length of the T-lines and the amplifier's output

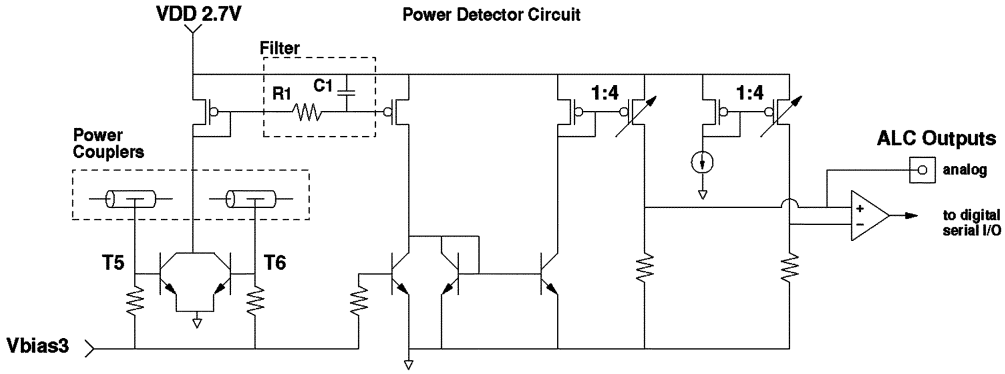

Fig. 7. Simplified power detector circuit schematic (bias circuits, voltage regulators, and serial interface omitted).

matching network remains unchanged. One capacitor is used in each output T-line which creates a differential detector voltage $V_{\rm ac}$. See Section III-A for more details on the physical coupler design.

The power detector circuit uses a pair of common-emitter (CE) HBT transistors (T5, T6) to convert the differential voltage swing $V_{\rm ac}$ into a current that is proportional to the amplifier's output power [13]. The transistors (1-μm long) are biased at 10 μA in a class-B regime where the device will be significantly nonlinear. As a result each collector current will show a host of harmonic and inter-modulation distortion components. Each collector current can be approximated by $I_C = I_0 e^x \approx I_0(1+x+x^2/2!+x^3/3!+\cdots)$, where $x = V_{\rm BE}/V_T$ has its usual meaning. The combination of both transistor currents will remove all odd-order distortions. The dominant even-order components, however, stay, and to the first order, make the sum of the collector currents proportional to the squared input voltage ($I_{C1+C2} \propto x^2$). Because of $x_0^2 \cos^2 i\omega t = x_0^2/2(1+\cos(2i\omega t))$, the square-law will produce mixing components at DC that can be low-passed filtered to produce a DC current that is proportional to true RMS power. See Fig. 7 for the location of the passive *RC* filter with a pole at 13.8 MHz ($R_1 = 27.2$ kΩ, $C_1 = 425$ fF).

The current is then multiplied and mirrored into an on-chip resistor to create an analog detector output voltage. Alternatively, the analog signal can be compared with a programmable 4-bit digital-to-analog converter (DAC) output to implement a successive approximation analog-to-digital converter (ADC) that can be read out via the chip's serial digital interface. Finally, a look-up table calibration is needed to provide an absolute power measurement. Note, the detector is linear with respect to the delivered output power $P_{\rm out} \propto V_{\rm ac}^2/R_L$. The square-law detection mechanism provides a true RMS power measurement, however, it assumes a constant load impedance R_L and the dynamic range of the detector is limited to this square-law region. If desired, the dynamic range could be extended with a series of cascaded detectors as described in [16]. Fig. 8 shows the measured analog detector output voltage at 60 GHz for the power sweep shown previously in Fig. 4. The detector shows a dynamic range from -5 to 12.5 dBm with a linear response from 4 to 12.5 dBm. The digital readout has a resolution of 2-dB per least-significant bit (LSB) in its linear region (0–12 dBm, not shown).

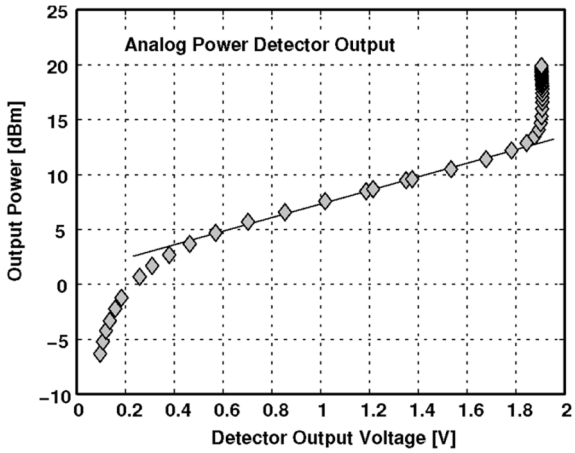

Fig. 8. Measured analog detector output voltage at 60 GHz for the power sweep show in Fig. 4.

In a BIST test-case the power detector readout can be used to test the amplifier without high-frequency probes and external test equipment. Each output pad simply needs to be terminated with a 50-Ω antenna or probe to provide accurate power readings. If, however, the PA is mis-terminated with a load impedance $Z_L \neq Z_0$ the readings will be off because of two reasons: 1) the output power delivered to the load changes according to

$$P_{\rm out} = P_0\left(1-\Gamma_L^2\right)$$

where

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{1}$$

is the reflection coefficient and Z_0 is the 50-Ω characteristic impedance of the on-chip transmission lines, and 2) the impedance seen by the power couplers has transformed according to

$$Z_L(l) = Z_0 \frac{Z_L + jZ_0 \tan\beta l}{Z_0 + jZ_L \tan\beta l} \tag{2}$$

where l is the distance between the power coupler to the location of the load Z_L. In our case, the load is only $l = 70$ μm

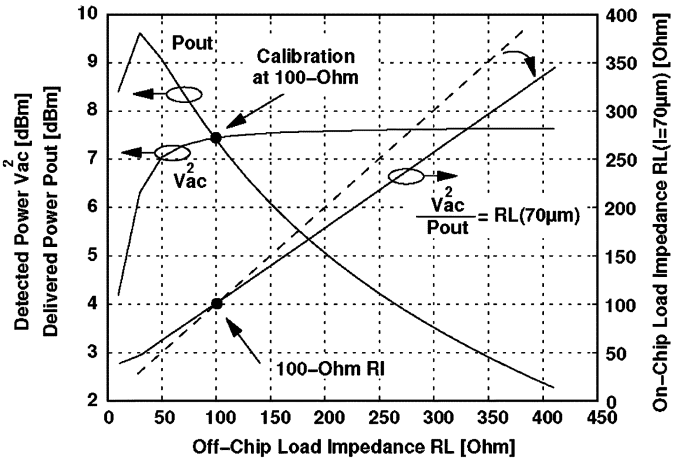

Fig. 9. Load-pull simulation of the PA and the power detector circuit for different load impedances $R_L = 10$–$400\ \Omega$. For impedances $Z_L \neq 100\Omega$ the calibrated power detector reading $(V_{\rm ac}^2)$ will change according to $V_{\rm ac}^2 = P_{\rm out} Z_L(l)$.

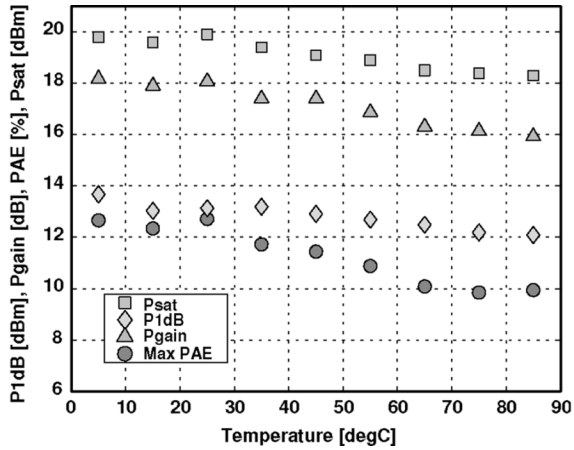

Fig. 10. Measured 60 GHz temperature variation without ALC control at constant current bias. The figure shows a 2-dB roll-off from 5–85 °C for P1 dB, $P_{\rm gain}$, and $P_{\rm sat}$. The PAE drops about 2% points. Note, for PVT-control the PA will have to run at a 2–3 dB back-off at room temperatures to provide enough headroom at elevated temperatures.

away from the contact pads and thus $Z_L(l)$ can be approximated with Z_L.

Fig. 9 shows a load-pull simulation of the PA and the power detector circuit for different load impedances $R_L = 10$–$400\ \Omega$. The figure shows that the delivered output power $P_{\rm out}$ drops according to (1) and the analog output from the detector increases because the impedance seen by the power coupler changes according to (2), where $l = 70\ \mu$m. Due to the 70 μm length offset, the fraction $V_{\rm ac}^2/P_{\rm out}$ is not directly proportional to Z_L (dashed line), but proportional to $Z_L(l)$. Note, for this simulation the detector circuit was calibrated at $R_L = 100\ \Omega$ to give exact $P_{\rm out}$ readings for 100-Ω load impedances.

Without the ALC circuit the amplifier is biased at constant current and its performance is PVT-dependent. This temperature dependence at 60 GHz is shown in Fig. 10. At 60 GHz P1 dB, $P_{\rm sat}$, and $P_{\rm gain}$ drop about 2 dB from 5–85 °C, while the PAE drops about 2% points. It can be seen that at room temperature, the power amplifier will have to run at 2–3 dB back-off to provide enough headroom for elevated temperatures.

A. mm-wave Power Coupler

The power coupler was designed to couple some energy from a T-line to the detector circuit, while having minimal effect on the T-line impedance. This makes the coupler electrically transparent with minimal reflections on the line. The 3-D structure of the device is shown in Fig. 11.

One coupler is integrated in each PA output T-line. A T-line has two side-shields on the top-layer metal and a ground-shield on the bottom-layer metal. The energy is coupled from the signal line by capacitive coupling into an intermediate metal-layer right between the signal line and the ground layer. The size of the capacitor impacts the dynamic range of the detector circuit and was choosen to give good sensitivity from 0–10 dBm. In order to balance the line impedance $Z_0 = \sqrt{L/C}$ locally, the inductance L in the coupler region was increased to compensate for the increase in capacitance C. This is done by opening a hole in the bottom shielding plane, which forces the return current to flow further away from the signal line thereby

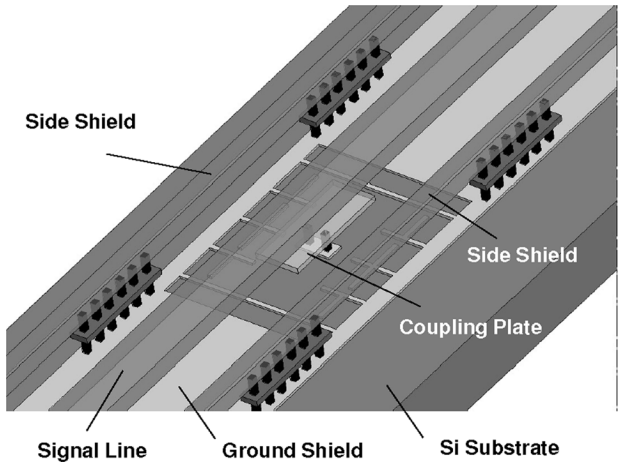

Fig. 11. Three-dimensional view of the physical HFSS [30] model of the power coupler used for full-wave electromagnetic simulations.

increasing the loop inductance and also reducing some of the capacitance to ground. A 2-D electromagnetic (EM) solver was used to obtain the impedance of the original T-line, and a 3-D EM solver was used to obtain the properties of the opened shield region. Some fill pattern has been added to the bottom shield hole area, which shields the fields from interfering with the power detector circuits below the T-line and from the silicon substrate. It should be noted that this sparse shielding wire pattern increases the capacitance of the metal plate to ground slightly.

Two design approaches have been considered: 1) the power coupler can be tuned to work best with a given input impedance of the power detector circuit, or 2) it can be designed to work reasonably well for a larger variety of power detector circuits. In the first approach, the metal plate length, the bottom shield opening, and the shielding wire pattern, make the effective impedance in the opened region exactly equal to the impedance of the T-line. In the second approach, a compromise in the design parameters can be used to minimizes the discontinuity in the T-line impedance for both, a grounded or a floating metal

TABLE I
COMPARISON OF SiGe mm-WAVE POWER AMPLIFIERS

Freq. [GHz]	Tech. [μm]	Mode [1]	Power[2] Comb.	P_{sat} [dBm]	GT_{sat}[3] [dB]	CP_{1dB} [dBm]	GT_{max}[4] [dB]	PAE_{peak} [%]	Reference
60	SiGe 0.13	diff. 100Ω	no	20	4.5	13.1	18	12.7	This Work
58	SiGe 0.13	singl. 50Ω	no	11.5	1	–	4.2	20.9	Valdes-Garcia [17]
60	SiGe 0.18	bal. 100Ω	no	15.8	–	11.2	11.5	16.8	Wang at al. [19]
61.5	SiGe 0.13	diff. 100Ω	no	14	6	8.5	12	4.2	Pfeiffer at al. [18]
77	SiGe 0.13	diff. 100Ω	no	18.5	–	–	–	5.4	Li at al. [21]
77	SiGe 0.13	singl. 50Ω	2x	17.5	12	14.5	17	12.8	Komijani at al. [22]
77	SiGe 0.13	diff. 100Ω	no	12.5	4.5	11.6	6.1	2.5	Pfeiffer at al. [20]
85	SiGe 0.13	singl. 50Ω	4x	21	5	–	8	3.4	Afshari at al. [23]

[1]Single-ended, differential, or balanced mode of operation
[2]On-chip power combining used
[3]Gain at saturation
[4]Maximum transducer power gain, or small-signal gain

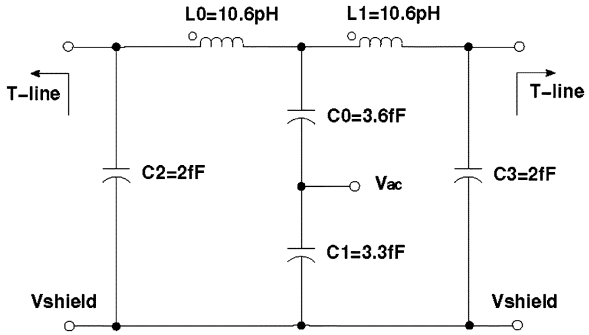

Fig. 12. Shows the equivalent circuit model that was used in circuit simulation. In the PA schematics it is located between two 50-Ω T-lines on both sides.

plate connection. The coupler plate then acts as an impedance divider with approximately equal impedance to the line and to the ground. It should be noted that in the opened region most of the return current flows in the side shields, and therefore, the shield cross section was made sufficiently large to avoid electro-migration effects.

Fig. 12 shows the equivalent circuit model of the power coupler. This equivalent circuit refers only to the hole region, since it is connected in the design schematics between two T-line devices on both sides. A one segment lumped model is justifiable since the length of the hole region is negligible compared with the wavelength. The resistive loss elements were not included due to the small loss of the short hole region. The electrical parameters of the hole region have been extracted from a larger region 3-D EM simulation where the 2-D properties of the T-lines on both sides have been subtracted.

IV. CONCLUSION

A single-stage differential cascode circuit topology was used to provide high gain, efficiency and output power at 60 GHz. The amplifier is intended to be used in multi-purpose *IQ* radios that can operate under various modulation schemes. The differential operation of the amplifier is used to lower the required impedance transformation ratio for differential antennas, which improves the efficiency of the output matching network. Center-tapped microstrip lines have achieved a compact layout to further lower losses related to the DC-resistance of long quarter-wave RF-chokes. The amplifier can provide an output power up to 20 dBm, which to date, is among the non-power-combining amplifiers the highest reported output power at mm-wave frequencies in a silicon process technology. For a comparison see Table I. The amplifier achieves a high level of integration which is unique for mm-wave frequencies, where a serial digital interface, programmable on-chip bias voltage generation, a power detector, and an automatic level control circuit was included on a single silicon chip. Future work will investigate other modes of operation to optimize the PAs linearity according to custom application and modulation schemes.

ACKNOWLEDGMENT

The authors would like to thank all who contributed to the fabrication of the chip, especially the IBM SiGe technology group at IBM Burlington, and DARPA. Special thanks goes to R. Carmon, IBM Haifa Research Laboratories, for EM modeling support, and V. W. Leung, S. Reynolds, B. Floyd, and A. Valdes-Garcia, IBM T. J. Watson Research Center, for helpful discussions. Much appreciation goes to B. Gaucher, M. Soyuer, and M. Oprysko of the Communications Department at the IBM T. J. Watson Research Center for their support of this work.

REFERENCES

[1] J.-S. Rieh, D. Greenberg, A. Stricker, and G. Freeman, "Scaling of SiGe heterojunction bipolar transistors," *Proc. IEEE*, vol. 93, no. 9, pp. 1522–1538, Sep. 2005.

[2] J.-S. Rieh, M. Khater, K. Schonenberg, F. Pagette, P. S. T. Adam, K. Stein, D. Ahlgren, and G. Freeman, "Collector vertical scaling and performance tradeoffs in 300 GHz SiGe HBTs," in *Proc. Device Research Conf.*, 2004, vol. 1, pp. 235–236.

[3] M. Khater, J.-S. Rieh, T. Adams, A. Chinthakindi, J. Johnson, R. Krishnasamy, M. Meghelli, F. Pagette, D. Sanderson, C. Schnabel, K. Schonenberg, P. Smith, K. Stein, A. Stricker, S.-J. Jeng, D. Ahlgren, and D. Freeman, "SiGe HBT technology with $f_{\max}/f_t$ = 350/300 GHz and gate delay below 3.3 ps," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, 2004, pp. 247–250.

[4] S. Reynolds, B. Floyd, U. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "Silicon 60 GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2830, Dec. 2006.

[5] B. Floyd, S. Reynolds, U. R. Pfeiffer, T. Beukema, J. Grzyb, and C. Haymes, "A silicon 60 GHz receiver and transmitter chipset for broadband communications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006, pp. 184–185.

[6] U. Pfeiffer, J. Grzyb, D. Liu, B. Gaucher, T. Beukema, B. Floyd, and S. Reynolds, "A chip-scale packaging technology for 60 GHz wireless chipsets," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 8, pp. 3387–3397, Aug. 2006.

[7] Y. Sun, S. Glisic, and F. Herzel, "A fully differential 60 ghz receiver front-end with integrated PLL in SiGe:C BiCMOS," in *Proc. European Microwave Integrated Circuits Conf.*, 2006, pp. 198–201.

[8] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, Y. Wang, and A. Hajimiri, "A 77 GHz phased array transmitter with local LO-path phase-shifting in silicon," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006, pp. 182–183.
[9] U. Pfeiffer and A. Valdes-Garcia, "Millimeter-wave design considerations for power amplifiers in a SiGe process technology," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 57–64, Jan. 2006.
[10] Y. Zhou and M. Y. Wah, "A wide band CMOS RF power detector," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, 2006, pp. 4228–4231.
[11] Q. Hu, Z. Liu, L. Yan, and W. Zhou, "A SiGe power amplifier with power detector and VSWR protection for TD-SCDMA application," in *Proc. Int. Conf. Mixed Design of Integrated Circuits and System*, 2006, pp. 214–217.
[12] M. Kouwenhoven and A. van Staveren, "A 2 GHz mean-square power detector with integrated offset chopper," *IEEE J. Solid-State Circuits*, vol. 1, no. 2, pp. 124–588, Feb. 2005.
[13] V. Leung, L. Larson, and P. Gudem, "Digital-IF WCDMA handset transmitter IC in 0.25-μm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2215–2225, Dec. 2004.
[14] S. Wong and S. Luo, "A 2.7–5.5 V, 0.2–1 W BiCMOS RF driver amplifier IC with closed-loop power control and biasing functions," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2259–2264, Dec. 1998.
[15] I. G. Y. Lu and A. Jenkins, "A closed-loop power control circuit for UWB 24 GHz automotive radar transmitter," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2006, pp. 1672–1675.
[16] T. Zhang, W. Eisenstadt, R. Fox, and Q. Yin, "Bipolar microwave RMS power detectors," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2188–2192, Sep. 2006.
[17] A. Valdes-Garcia, S. Reynolds, and U. R. Pfeiffer, "A 60 GHz Class-E power amplifier in SiGe," in *Proc. Asian Solid-State Circuits Conf.*, 2006, pp. 199–202.
[18] U. R. Pfeiffer, D. Goren, B. A. Floyd, and S. K. Reynolds, "SiGe transformer matched power amplier for operation at millimeter-wave frequencies," in *Proc. European Solid-State Circuits Conf. (ESSCIRC)*, 2005, pp. 141–144.
[19] C. Wang, Y. Cho, C. Lin, H. Wang, C. Chen, D. Niu, J. Yeh, C. Lee, and J. Chern, "A 60 GHz transmitter with integrated antenna in 0.18 μm SiGe BiCMOS technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006, pp. 186–187.
[20] U. Pfeiffer, S. Reynolds, and B. Floyd, "A 77 GHz SiGe power amplifier for potential applications in automotive radar systems," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig. Papers*, 2004, pp. 91–94.
[21] H. Li, H.-M. Rein, T. Suttorp, and J. Boeck, "Fully integrated SiGe VCOs with powerful output buffer for 77 GHz automotive radar systems and applications around 100 GHz," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1650–1658, Oct. 2004.
[22] A. Komijani and A. Hajimiri, "A wideband 77 GHz, 17.5 dBm power amplifier in silicon," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2005, pp. 566–569.
[23] E. Afshari, H. Bhat, X. Li, and A. Hajimiri, "Electrical funnel: A broadband signal combining method," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006, pp. 206–207.
[24] U. R. Pfeiffer, "A 20 dBm fully-integrated 60 GHz SiGe power amplifier with automatic level control," in *Proc. European Solid-State Circuits Conf. (ESSCIRC)*, 2006, pp. 356–359.
[25] U. R. Pfeiffer, "Low-loss contact pad with tuned impedance for operation at millimeter wave frequencies," in *Proc. 9th IEEE Workshop on Signal Propagation on Interconnects*, 2005, pp. 61–64.
[26] T. Zwick and U. R. Pfeiffer, "Pure-mode network analyzer concept for on-wafer measurements of differential circuits at millimeter wave frequencies," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 3, pp. 934–937, Mar. 2005.
[27] J. Grzyb, D. Liu, U. Pfeiffer, and B. Gaucher, "Wideband cavity- backed folded dipole superstrate antenna for 60 GHz applications," in *Proc. IEEE Int. Symp. Antennas and Propagation*, 2006, pp. 3939–3942.
[28] G. F. Knoll, *Radiation Detection and Measurement*, 3rd ed. New York: Wiley, 2000.
[29] V. Milanovic, M. Gaitan, E. Bowen, N. Tea, and M. Zaghloul, "Thermoelectric power sensor for microwave applications by commercial CMOS fabrication," *IEEE Electron Device Lett.*, vol. 81, no. 9, pp. 450–452, Sep. 1997.
[30] High frequency structure simulator (HFSS), version 9. Ansoft Corp., Pittsburgh, PA.

Ullrich R. Pfeiffer (M'02–SM'06) received the diploma degree in physics and the Ph.D. in physics from the University of Heidelberg, Germany, in 1996 and 1999 respectively.

In 1997, he worked as a Research Fellow at the Rutherford Appleton Laboratory, Oxfordshire, U.K., where he developed high-speed multi-chip modules. In 2000, his research was based on real-time electronics for a particle physics experiment at the European Organization for Nuclear Research (CERN), Switzerland. From 2001 to 2006, he was with the IBM Thomas J. Watson Research Center where his research involved RF circuit design, power amplifier design at 60 GHz and 77 GHz, high-frequency modeling and packaging for millimeter-wave communication systems. Since 2007, he has been the head of the THz electronics group at the Institute of High-Frequency and Quantum Electronics at the University of Siegen, Germany.

Dr. Pfeiffer is a member of the German Physical Society (DPG). He was the co-recipient of the 2004 and 2006 Lewis Winner Award for Outstanding Paper at the IEEE International Solid-State Circuit Conference. He received the European Young Investigator Award in 2006.

David Goren (M'01) received the B.Sc. and M.Sc. degrees, and in 1998, the Ph.D. degree, in electrical engineering, from the Technion, Haifa, Israel, specializing in semiconductor device physics and microelectronics.

In 1997, he joined IBM and is presently a Research Staff Member at the IBM Haifa Research Laboratories, Haifa, Israel, in the general field of analog and mixed-signal design research. He is currently the technology leader (and founder) of the IBM On-Chip T-line project, for which he received an IBM outstanding innovation award in 2003, and whose products have been integrated within IBM technology design kits since 2001. Since 1998, he has also been a Lecturer and graduate student advisor in the Technion. He has published 30 papers (IEEE and Applied Physics) and holds 12 patents.