A 1V fully integrated CMOS transformer based mixer with 5.5dB gain, 14.5dB SSB Noise figure and 0dBm input IP3

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Abstract

A fully integrated low voltage mixer topology is presented. The problem of stacking input-, cascode- and switching-transistors within 1V supply voltage is solved by inserting a transformer, optimized for high coupling and high self-resonance frequency. A fully integrated testchip aiming at UMTS applications around 2GHz to demonstrate the feasibility was manufactured in INFINEON low-cost 0.13μm 6 metal standard CMOS process. The single-ended mixer, including the on chip resistive 50 Ω termination, features a gain of 5.5dB, a SSB Noise figure of 14.5dB, an input IP3 of 0dBm and an input 1dB compression point of -10 dBm consuming 40 mW at a power supply voltage of 1 V. The mixer 3dB-bandwidth ranges from 1.3 GHz up to 4.1GHz.

1. Introduction

The ongoing technology down-scaling increases continuously the attractiveness of RFCMOS transceivers as the high frequency capability meanwhile largely exceeds the frequency of popular GSM, UMTS or WLAN applications. E.g. a modern 0.13 μm standard CMOS process [1] features an f_T of ca. 100GHz enabling highly integrated transceivers as demonstrated e.g. for UMTS-applications in [2,3]. The decreasing power supply voltages with the technology downscaling however leads to severe circuit design problems. The nominal power supply voltage of e.g. 1.5 V of 0.13 μm CMOS severely limits the possibility of transistor stacking. Common designers practice of using cascode structures becomes nearly impossible. Especially the widely used gilbert mixer cell [4] becomes severe linearity problems due to the large number of stacked transistors. Other very linear mixer topologies, better suited for low-voltage operation, exist [5, 6] but feature poor noise figure and/or conversion gain. This paper proposes the insertion of a transformer into the classical Gilbert mixer, extending its operation down to very low supply voltages.

2. Design

Fig. 1 introduces the principle of the proposed transformer based mixer topology. On the left hand side, the conventional structure is shown, the right side shows the insertion of the transformer. For simplicity a single ended commutating mixer is used. For better linearity and backwards isolation a cascode transistor is inserted on top of the input transistor.

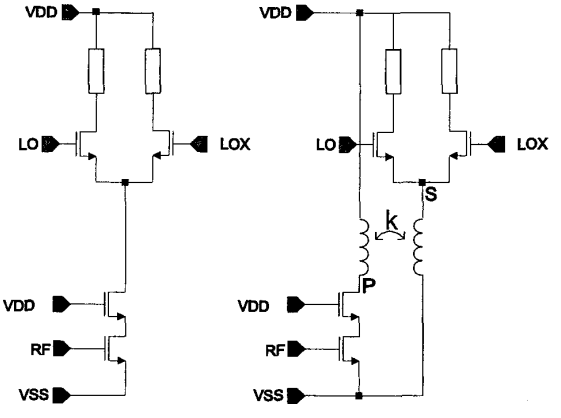

Figure 1. Left: conventional mixer topology, Right: proposed transformer based mixer topology

Trivially a four quadrant mixer can be deviated from this schematic when drawing (and layouting) it twice. The discussion and demonstration of the concept in this paper however is limited to the single-ended version.

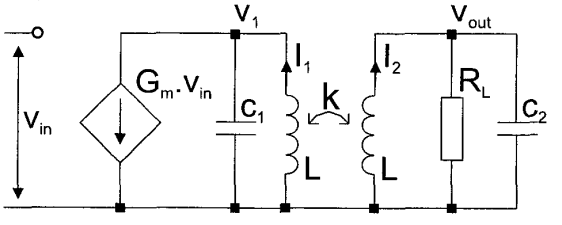

Figure 2. Small signal mixer model

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Neglecting the cascode stage, the transformer based mixer can be modeled by the small signal model shown in Fig. 2. g_m is the transconductance of the RF input transistor, R_L is the output load, C_1 and C_2 represent the parasitic capacitances at the input and output node of the transformer. The transformer is assumed symmetrical with equal input and output inductance L and coupling factor k. Writing down Kirchoff's equations, leads to the transfer function:

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{\frac{1+\omega^2 C_1 L}{kj\omega L}(1 - \frac{j\omega L}{R_L} + \omega^2 C_2 L) + k\omega^2 L C_1 \frac{1+j\omega C_2 R_L}{R_L}} \quad (1)$$

which for $C_1 = C_2 = 0$ reduces to

$$\frac{v_{out}}{v_{in}} = \frac{kg_m}{\frac{1}{j\omega L} - \frac{1}{R_L}} \quad (2)$$

Eqn. (2) leads to the trivial conclusion that the coupling factor k should be maximized, and that the output voltage is maximized for higher inductance values. Eqn. (1) is more difficult to interpret, but it also leads to a rather trivial observation that C_1 and C_2 should be minimized so that the AC-currents flow through the inductors. These requirements, i.e. high k and low capacitances, are ideally met by the staggered symmetrical coil, as discussed for VCO-designs in [7]. The middle connection of the symmetrical coil is cut through, one side is connected to VDD, one side is connected to VSS. The smaller and shorter inner windings of the coil feature minimal parasitic capacitances and are used as the primary (node S in Fig. 1 and 5) and secondary connections (node P in the same Fig.'s) of the transformer. Furthermore the coupling factor of the coil benefits from the compact staggered layout. FASTHENRY [8] simulations revealed a coupling factor as high as 0.8 for the 5 windings coil visible from the chip photograph (Fig. 5).

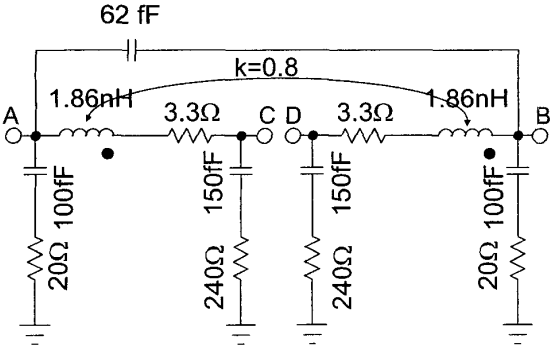

Figure 3. Estimated coil model

The coil model, estimated from FASTHENRY simulations and s-parameter measurements of the structure with nodes C and D shorted, is presented in Fig. 3. Nodes A and B correspond to nodes S and P in Fig. 1. Nodes C and D are connected to VSS and VDD in Fig. 1. To reduce the series resistances of the windings metal 4, 5 and 6 were used in parallel. Based on this coil, a single-ended mixer testchip was manufactured in INFINEON 0.13 μm standard CMOS with 6 copper levels. The schematic of the testchip including on-chip resitive 50Ω termination and the measurement setup is shown in Fig. 4.

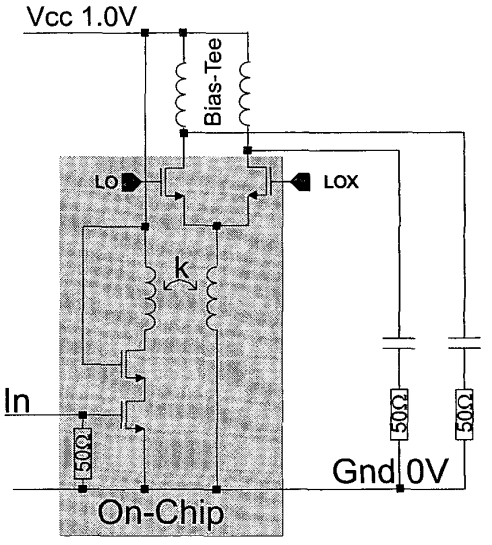

Figure 4. Mixer testchip schematic and measurement setup

Main difference to the principle schematic is the resistive on-chip termination to enable reliable measurements in 50Ω systems,although deteriorating the conversion gain by ca. 3dB.

3. Measurements

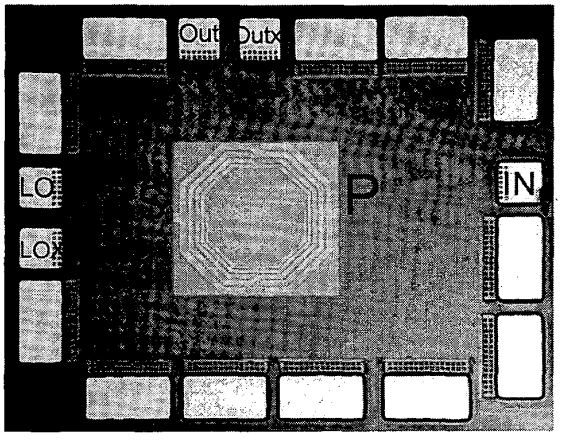

Figure 5. Mixer testchip photograph

The chip photograph is shown in Fig. 5. Die size is 630μm by 800μm, coil size is 240μm by 240μm. All measurements were done at 1V supply voltage, power con-

sumption was 40mA. Mixer linearity was measured for an LO input frequency of 2GHz and an RF input frequency of 2.15GHz, aiming at mobile UMTS applications. The one tone compression measurement is presented in Fig. 6. 1-dB input compression point is -10dBm.

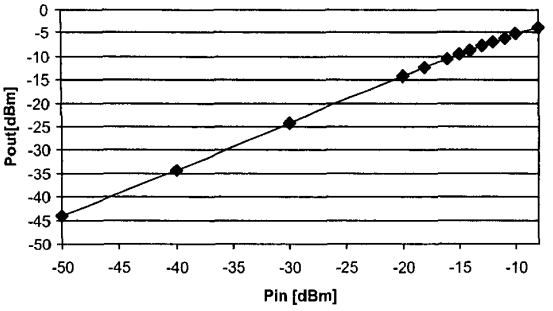

Figure 6. Mixer compression, LO 2.0GHz 3dBm, RF 2.15GHz

Two tone intermodulation measurements are presented in Fig. 7 and 8. The distance between the tones of 1MHz again is deviated from typical UMTS applications. The 1V mixer features a measured input IP3 point of 0dBm.

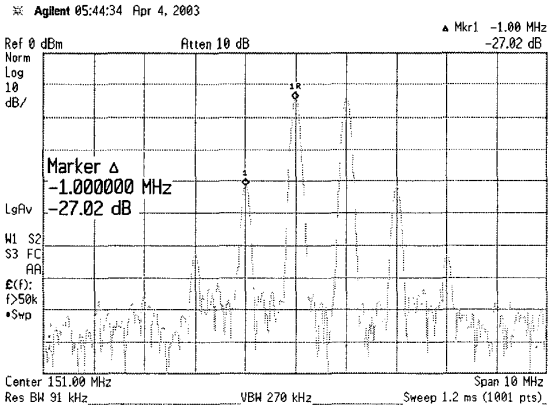

Figure 7. Mixer two tone test output spectrum for LO 2.0GHz 3dBm and RF 2.150GHz & 2.151GHz both -13.7dBm

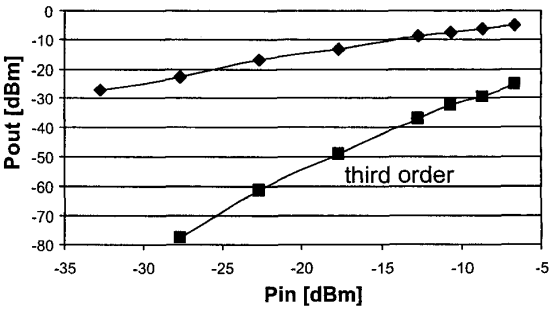

Figure 8. Mixer two tone test, LO 2.0GHz 3dBm, RF 2.150GHz & 2.151GHz

Noise figure was also measured at 2.15GHz RF input frequency and 2.0GHz LO frequency using Agilent E4448A spectrum analyzer and a low-noise pre-amplifier. The measured SSB noise figure is 14.5dB. The frequency range of operation of the mixer was measured sweeping RF- and LO-input frequency with a constant offset of 150MHz. The result is presented in Fig. 9. Although transformer based, the mixer features a remarkable high bandwidth which is probably due to the optimized coil layout with high coupling factor and low capacitances.

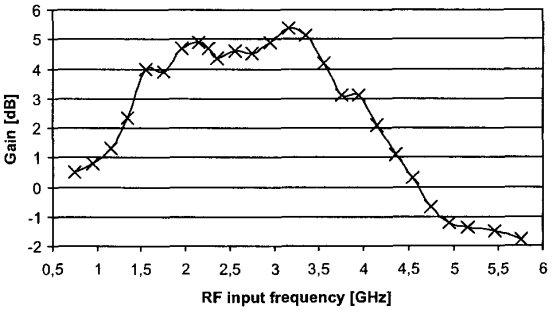

Figure 9. Mixer Gain over frequency, LO power 3dBm, fixed output frequency 150MHz

The mixer characteristics are summarized in Table. 1.

4. Summary

A transformer based mixer topology is proposed to extend the use of classical commutating mixers to very low supply voltages. The transformer is realized as an optimized symmetrical with staggered winding width because of its high coupling and low parasitic capacitances. A fully integrated mixer testchip aiming at 2GHz UMTS applications was manufactured in INFINEON low-cost 0.13μm 6 metal standard CMOS process and verifies the power of the transformer concept. At 2GHz, the single-ended mixer, including the on chip resistive 50Ω termination, features a measured gain of 5.5dB, an SSB Noise figure of 14.5dB, an input 1dB compression point of -10dBm and an input IP3 intermodulation point of 0dBm consuming 40mW at a power supply voltage of 1V.

Table 1. mixer summary, nominal operation at 2GHz LO freq. and 2.15GHz RF freq.

Power supply	1.0 V
Power consumption	40 mW
Gain	5.5dB
SSB Noise Figure	14.5dB
Input compression point	-10 dBm
Input IP3	0 dBm
3 dB Bandwidth	1.3-4.1 GHz
Technology	0.13 μm standard CMOS

5. References

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