60-GHz Single-Chip Integrated Antenna and Low Noise Amplifier in 65-nm CMOS SOI Technology for Short-range Wireless Gbits/s Applications

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***Abstract*— The single-chip integration of antenna and Low Noise Amplifier (LNA) for 60 GHz short-range wireless transceivers is presented in this work. A 65 nm CMOS Silicon-on-Insulator (SOI) technology has been selected as target; due to its high-resistivity substrate the losses are drastically reduced if compared with the bulk silicon technology and more energy will be provided to the on-chip antenna to radiate. Two different LNA architectures are proposed. First, a three-stage LNA with conventional 50 Ohm input matching allows for a power gain of 23 dB, a noise figure (NF) of 4.04 dB and a power consumption of 35 mW. By relaxing the impedance matching specification, due to on-chip co-design of amplifier and antenna, a new LNA with only two amplification stages has been designed. The two-stage LNA achieves similar performance of the three-stage one (gain >22 dB, NF< 5 dB) with a power consumption reduced by 25%. A dipole antenna with coplanar strip feed has been also designed matching the input LNA impedance and allowing an antenna gain of 3.22 dB at 60 GHz with a limited on-chip area occupation.**

***Index Terms*— 60-GHz, CMOS Silicon On Insulator (SOI), LNA (low-noise amplifier), Integrated antenna, Wireless Gbits/s**

I. Introduction

In telecommunications, networking and consumer electronics fields there is a growing interest for short-range wireless communications with high bandwidth capabilities, up to several Gbits/s. The availability of low-power RF transceivers with such high data-rate will enable new wideband and interoperable communication services among consumer electronics, personal computing and mobile devices such as wireless fast internet access, uncompressed video communication, wireless USB connections, wireless video area networks connecting devices such as TV decoders, DVD readers, videocameras, game consoles.

To this aim new standards are under development and new consortium of academia and industries have been created such as the WirelessHD [1,2], based on the IEEE 802.15.3c standard for multi-gigabit WPAN, or the WiGig alliance [3-5], starting from the IEEE 802.11ad standardization effort.

At physical layer such standards exploit the unlicensed multi-GHz band allocated world-wide around 60 GHz, see Fig. 1. As example the Federal Communications Commission (FCC) allocated a 7-GHz band in the radio frequency spectrum between 57 and 64 GHz [6]. Other countries worldwide have allocated the 60-GHz band for unlicensed wireless communications (Australia [7], Korea [8], Europe [9]), allowing a universal compatibility for the system operating in a band of 3 GHz.

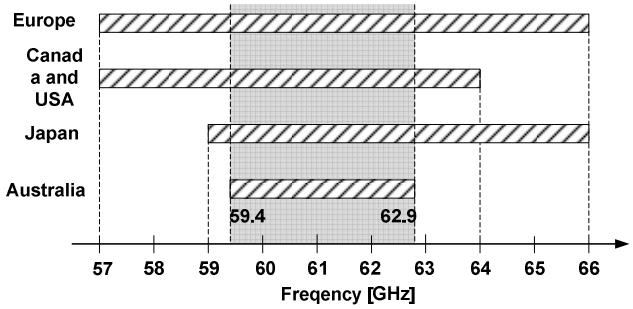

Fig. 1. Table of frequency allocation around 60 GHz.

Recent advances in silicon technologies allow to implement integrated transceivers operating at millimeter-waves enabling the realization of a new class of mass-market devices for very high data rate communications [10]. Current research in academia and industry is focused on the design of integrated transceivers in CMOS or CMOS Silicon-on-Insulator (SOI) technologies to minimize power consumption and size. With respect to III-V or SiGe technologies for millimeter-wave applications the CMOS approach is promising to reduce terminal cost in case of large volume applications and in case of close integration of RF and digital circuitry.

CMOS transceivers for 60 GHz applications have been recently proposed in literature [10-13] while the antenna is typically realized off-chip and a 50-Ohm input impedance is used during the Low Noise Amplifier (LNA) design. However at 60 GHz there is the possibility of integrating on-chip also the antenna thus further reducing the system size. To this aim the 65-nm SOI technology is the most promising one.

With respect the state of the art this work presents the design of an on-chip integrated antenna and LNA in 65-nm CMOS SOI technology from STMicroelectronics. When using the on-chip antenna some constraints of the LNA design, e.g. 50-Ohm input impedance, can be removed and hence the design space exploration becomes a key issue to find if new LNA architectures vs. state of the art can be found with better trade-off between gain, noise figure and power consumption.

The rest of the paper is organized as follows. Section II presents a system-level analysis carried out to define the re-

quirements for the gain of the LNA plus antenna design. Section II also presents the CMOS SOI technology and its use for millimeter-wave design. Section III presents and compares the design and characterization by simulations of two different LNA circuit architectures implemented in 65 nm CMOS SOI. The design of a dipole integrated antenna in the same technology, matched with the proposed LNAs, is discussed in Section IV. Conclusions are drawn in Section V.

II. Antenna and LNA Requirements for 60-GHz Fully Integrated Receiver

A. Antenna and LNA gain specification

The first step for the definition of the LNA and antenna architecture is specifying their target requirements in terms of antenna gain and in terms of LNA gain and noise figure. Being the antenna and the LNA integrated on-chip the requirement on the impedance matching is released since the achievement of 50 Ohm is not mandatory.

$$S_{RX} = 10xLog_{10}KTB + SNR_{dB} + NF_{dB} \quad (1)$$

From equation (1) considering a receiver sensitivity of -50 dBm (as in WirelessHD [11] and above the minimum -60dBm of ECMA-387 [14]), a bandwidth of 3 GHz around the 60 GHz, and a required SNR of roughly 20 dB (to have a low BER of $4x10^{-11}$ as in [11]) then the Noise Figure (NF) must be less than 10 dB.

Considering the Friis formula for path losses estimation, with the hypothesis of using the same antenna for transmitter and receiver and under the assumptions of a target distance of few meters (within 10 m), of a power transmission of 10 dBm and a sensitivity of -50 dBm as in [11][1], then the gain of the antenna plus the LNA should be around 20 dB. If we set the LNA gain at 20dB then, in the above considered conditions, Fig. 2 details the required antenna gain vs. the connection distance.

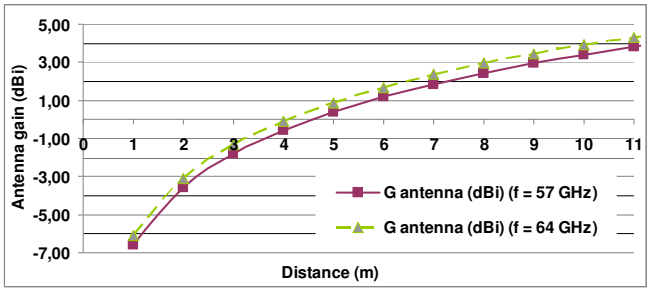

Fig. 2. Antenna gain requirement as a function of connection distance.

Summarizing, an LNA with a gain of 20 dB and a NF below 10 dB and an on-chip antenna with a gain of few dBi are needed for short-range multi-gigabit communication. The low antenna gain specification is compatible with the requirement of an antenna with a large irradiation angle useful when creating consumer devices networks.

As far as the selection of the target technology is concerned, Section II.B reviews the use of CMOS SOI as a promising alternative in consumer markets vs. SiGe BICMOS and III-V HBT/ HEMT technologies and with better performance vs. bulk-CMOS.

[1] In ECMA-387 [14] a power transmission of 0 dBm and a sensitivity of -60 dBm can be considered but the result is the same.

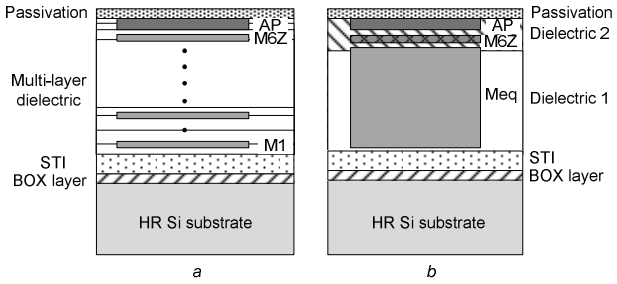

Fig. 3. *a)* Cross section of SOI CMOS back-end and *b)* Simplified cross-section of SOI CMOS back-end for 3D-EM simulations.

B. SOI CMOS: Technology description and cross section

The SOI CMOS technology shows very attractive performance for the millimeter-wave system-on-chip design, since the high active performance of MOS transistors are combined with the high-resistivity (HR) of the SOI substrate. Indeed, the feature that the circuit elements are isolated dielectrically allows the SOI technology to significantly reduce junction capacitances and the circuits to operate at high speed or substantially with lower power at the same speed. Moreover, the device structure also eliminates the latch-up in bulk CMOS and improves the short channel effect immunity. A cross section of the CMOS SOI technology is shown in Fig. 3a, in which the buried oxide (BOX) layer ($\varepsilon_r = 4$) and the high resistive (HR) substrate ($\varepsilon_r = 11.7$, $\sigma_{Si} = 0.0001$ S/m, and $h_{Si} = 355\ \mu m$) can be noted.

In this technology the back-end consist of a very complex multi-layer in which the dielectric multi-layer is composed by an alternation of SiO_2 and Si_2N_4. For computing time reasons, since the 3D-EM simulator used is a volume field solver, the multi-layer back-end has been simplified to an equivalent back-end with thick layers that results in a more efficient solution. In detail, the parameters to take into account in order to build the simplified cross-section of the SOI CMOS process are the metallization thickness made of 6 thick copper staked layers (M_1-M_{6Z}), the aluminum capping layer (AP) and the multi-layer dielectrics. The simplified cross-section for the 3D-EM simulations are reported in Fig. 3b. It is worth noting that the multi-layer stack can be significantly compressed without compromising the accuracy. For that purpose, a weighted average of the dielectric material properties and thickness calculated has been applied. The relative permittivity of each equivalent layer ($\varepsilon_{r,eq}$) is calculated by:

$$\varepsilon_{e,eq} = \left[\sqrt{\varepsilon_n} + \frac{h_{n-1}}{h_{n-1}+h_n}\left(\sqrt{\varepsilon_{n-1}} - \sqrt{\varepsilon_n}\right)\right]^2 \quad (2)$$

where n is the layer index, ε_n and h_n are the relative permittivity and the thickness of the n^{th} layer, respectively.

Finally, as regard passive structures, the feasibility of transmission lines and antennas in SOI CMOS technology have been reported in [15,16]. In particular, the performance of the antennas designed in SOI CMOS process is better than

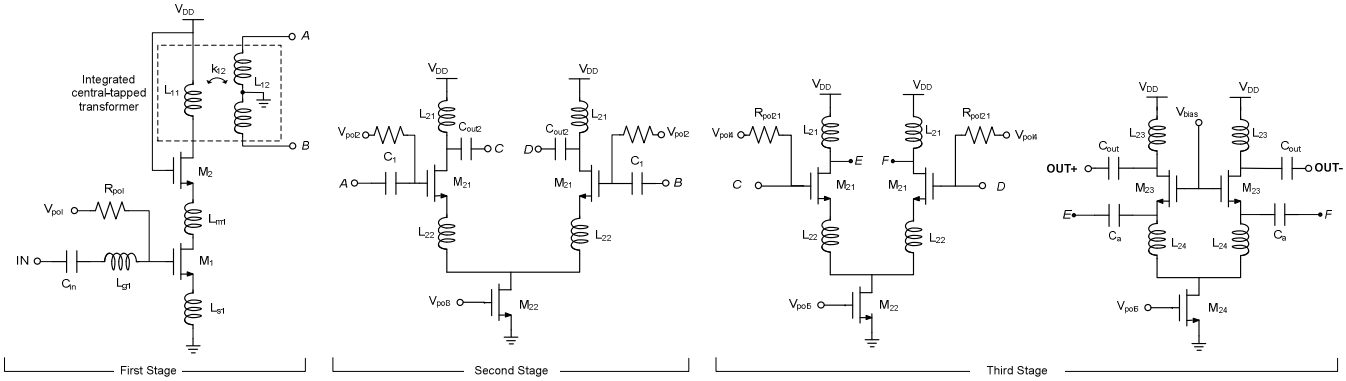

Fig. 4. Schematic of the 60-GHz three-stage LNA with 50-Ω input and output matching.

the same on standard CMOS process due to a reduced amount of energy stored in the supporting substrate. Hereafter two different LNAs plus an on-chip CPS (CoPlanar Strip) dipole antenna are proposed.

III. LNA DESIGN IN 65 NM CMOS SOI

In this section the design of two LNAs for the 60-GHz band are presented and debated. The design choices and the simulation results at schematic level are compared. The first LNA, in Fig. 4, has been designed by means of three amplification stages and by considering 50-Ω input impedance and a differential output, for the subsequent double balanced mixer, with a load impedance of 100 Ω. The second LNA, in Fig. 5, has been designed to reach the maximum in terms of power gain and noise figure without taking into account the values of input impedance. It was possible due to the fact that the antenna is integrated in the same chip, therefore the matching between antenna and LNA can be obtained by a proper dimensioning of the antenna, as shown in Sec.IV. By this way it has been possible to design a LNA with only two amplification stages capable to reach the desired power gain and noise figure, allowing a reduced power consumption and circuit complexity if compared to the three stage LNA.

A. *Three-stage LNA*

The three-stage LNA has been adopted to reach the specifications in terms of noise figure and power gain and the input and output matching (50 Ω and 100 Ω for the single input and differential output, respectively). Its schematic in Fig. 4 includes: i) a single-ended cascade stage, ii) a fully differential stage and iii) a fully differential cascode stage, modified vs. conventional solutions in order to remove the staked transistor (common-source and common-gate) and thus reducing the problems coming from low supply voltage in scaled technologies (1.2V of supply voltage in 65-nm CMOS technology). In detail, the first stage has been implemented in accordance with the power-constrained integrated input matching technique and with a MOSFET linear current density close to 0.15 mA/μm according to the latest advances in LNA design for the best noise figure [17,18]. Moreover, the first stage provides a proper differential output signal through an integrated inter-stage transformer for the fully differential second stage of amplification. The integrated transformer allows the transition from the single-ended (unbalanced) signal available from the first stage (i.e. from the antenna) to a proper differential output (balanced) for the subsequent double balanced mixer. The symmetric integrated inter-stage transformer has been properly designed by means of 3-D EM simulator (HFSS by Ansoft) in order to provide the maximum power delivery from the first to the second stage of the LNA in accordance with the design methodology in [19]. As recommended therein, the figure of merit for the integrated inter-stage transformer, called *'transformer characteristic resistance'*, has been maximized:

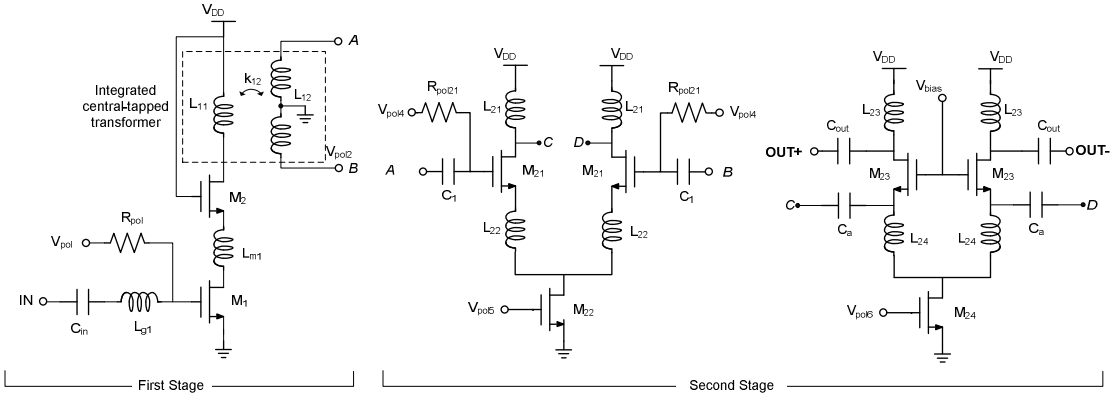

Fig. 5. Schematic of the 60-GHz two-stage LNA without 50-Ω input and output matching.

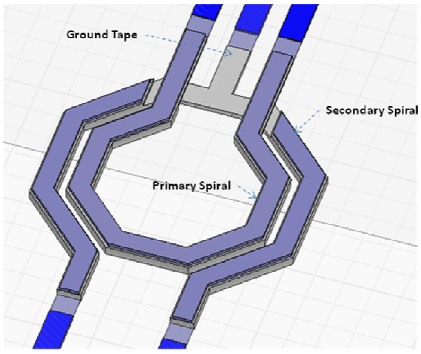

Fig. 6. Integrated inter-stage transformer.

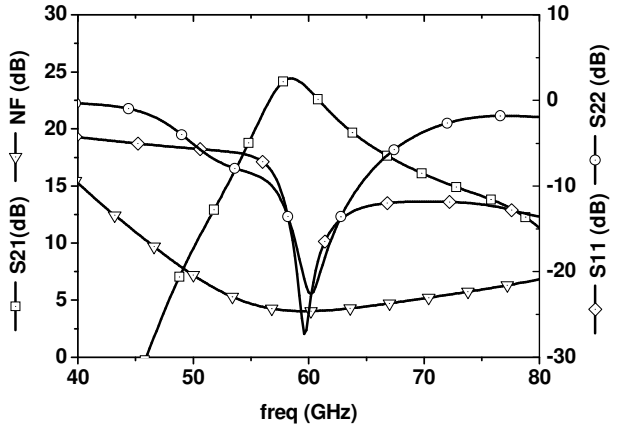

Fig. 7. Simulation results of the 60-GHz three-stage LNA: power gain, noise figure and input (S11) and output (S22) matching.

$$\zeta = \omega Q_{TP} L_{TP} \left(1 + k^2 \frac{Q_{TS}}{Q_{TP}}\right) \quad (3)$$

where L_{TP} is the inductance of the primary spiral, k is the coupling factor, and Q_{TP} and Q_{TS} are the quality factor of the primary and the secondary spiral of the transformer.

In particular, the transformer consists of two octagonal and symmetrical coupled planar inductors, both with 26 µm of diameter, one turns each, 3 µm spaced and 8 µm wide, as shown in Fig. 6. The structure has been designed by using all the metal layers available in the technology (M1-AP). Near to the intersection the first spiral has been designed in M6Z and AP, whereas the secondary spiral in M1-M5. It is worth nothing that this structure do not need under-pass reducing the parasitic effects due to the vias.

The primary spiral exhibits a self-inductance (L_{TP}) of 250 pH with an associated quality factor (Q_{TP}) [20] equal to 11, whereas the secondary spiral exhibits the same self-inductance (L_{TS} = 175pH) with a Q_{TS} equal approximately to 30, at 60 GHz.

The second fully-differential amplification stage in Fig. 4 allows the increase of the power gain and the benefits of the common mode rejection ratio (CMRR). Finally the third stage is a fully differential cascode converted into a common-source and common-gate stages (as shown in the Fig. 4) in order to have only two staked transistors between V_{DD} and GND. In fact in the new generations of standard silicon processes, especially as far as the CMOS is concerned, the trend is to reduce the voltage supply. By following this trend circuits with maximum two staked transistor are highly desired.

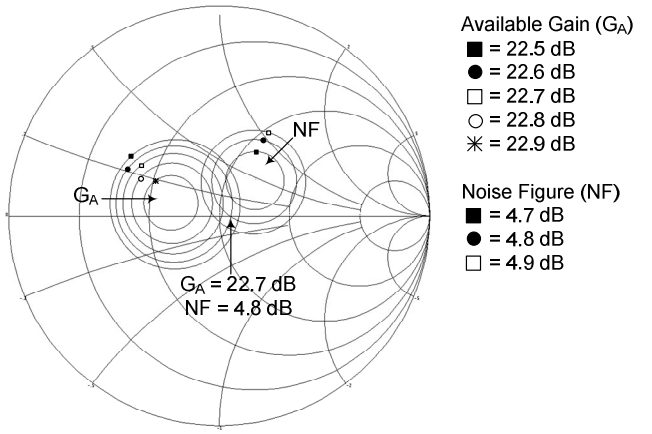

Fig. 8. Equi-G_A and equi-noise circles for the first stage of the 60-GHz two-stage LNA

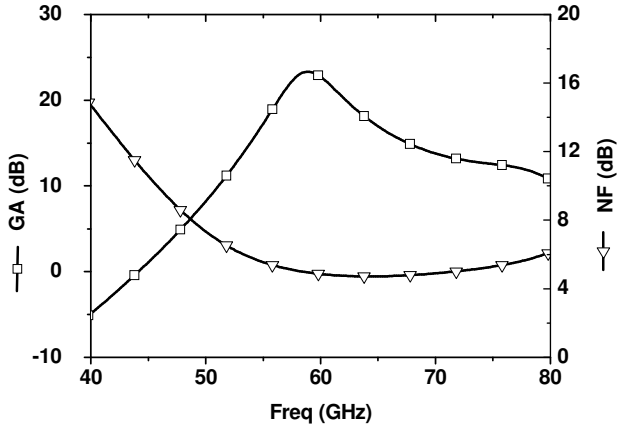

Fig. 9. Simulation results of the 60-GHz two-stage LNA: power gain and noise figure.

The final circuit exhibits a power gain of 23dB, a noise figure of 4 dB at 60GHz, as shown in Fig. 7. The input and output matching in terms of S-parameters amount to 26.56 dB (i.e. S11) and –21.56 dB (i.e. S22), respectively (see Fig. 7). As for the stability, the K factor is always greater than 10. The total power consumption is equal to 34.9 mW with a 1.2-V supply voltage.

B. Two-stage LNA

As described before, the two-stage LNA in Fig. 5 has been designed to reach a better trade-off among different performance metrics (power consumption, circuit complexity, power gain and noise figure) without taking into account a predefined constraint on the input and output impedances. To do this, the LNA has been implemented by considering the typical approach of microwave and millimeter-wave design. In detail, fixed the MOSFET current density close to 0.15 mA/µm [17,18] (for both stages), the equi-G_A and equi-noise circles have been used to reach a compromise between the power available gain (G_A) and the minimum noise figure. The LNA is composed by: i) a single-ended cascade stage, ii) a fully differential cascade stage modified in order to remove the staked transistor as described in the previous section. The

full schematic of the two-stage LNA is shown in Fig. 5. Also in this case the first stage provides a proper differential output signal to the fully differential second stage of amplification through an integrated interstage transformer that provides, in addition, the maximum power delivery from the first to the second stage of the LNA [19]. The transformer consists of two octagonal and symmetrical coupled planar inductors, both with 24 μm of diameter, one turns each, 3 μm spaced and 6 μm wide. The primary spiral exhibits a self-inductance (L_{TP}) of 183 pH with an associated quality factor (Q_{TP}) [20] equal to 15, whereas the secondary spiral exhibits the same self-inductance (L_{TS} = 147 pH) with a Q_{TS} equal approximately to 30, at 60 GHz. The second stage is a fully differential cascode, that allows the increase of the power gain and the benefits of the common mode rejection ratio (CMRR), converted into a common-source and common-gate stages (as shown in the Fig. 5) in order to have only two staked transistor between V_{DD} and GND. In Fig. 8 are shown the equi-G_A and equi-noise circles at 60 GHz for the first and the second stage of the LNA. In particular an input (Z_{IN}) and output (Z_{OUT}) impedances of 20 Ω and (57.5+j358.5) Ω respectively, have been considered. The circuit exhibits a power gain of 22.73 dB and noise figure of 4.86 dB at 60GHz as shown in Fig. 9. As for the linearity and the stability, the K factor is always greater than 4. The total power consumption is equal to 26.6 mW with a 1.2-V supply voltage.

Compared to the three-stages LNA this solution allow us to reach the same performance with only the 76% of the power consumption of the 3-stages LNA. Moreover in this solution there are 11 integrated inductors compared to the 16 inductors in the 3-stages LNA. This entail that the 2-stages LNA will occupy less area on die if compared to the 3-stages LNA.

Finally, the comparison with the most relevant CMOS solutions of the literature [21]-[27] in the 60 GHz frequency range is summarized in Table I. The proposed LNAs show the highest power gain with an associated moderate power consumption, especially if compared with the other differential LNAs, and a noise figure that is very close to the best values of the literature.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

	Process (CMOS)	**Topology**	**Gain [dB]**	**NF [dB]**	**Power [mW]**	**Work Freq. [GHz]**
Our 3-stage	*65nm SOI*	*3-stage diff. casc.*	*23.2*	*4.04*	*34.9*	*60*
Our 2-stage	*65 nm SOI*	*2-stage diff. casc.*	*22.8*	*4.86*	*26.64*	*60*
[21]	65 nm SOI	3-stage cascode	20.5	6.5	20	*60*
[22]	65 nm	2-stage cascode	22.4	4.5	16.8	*56*
[23]	250 nm SiGe BiCMOS	3-stage diff. CS*	18	6.8	66	*60*
[24]	130 nm	3-stage diff. CS*	15.9	3.7	N/A	*62*
[25]	65 nm SOI	2-stage CS*	12	8	36	*64*
[26]	65 nm	2 casc. + 1 CS*	22.3	6.1	35	*60*
[27]	45 nm	2 cascode	26	6	23	*60*

[*] Common Source

IV. SINGLE-CHIP CMOS SOI ANTENNA DESIGN

According to discussions in Section II.B the CMOS SOI technology is a good candidate to design the on-chip antennas for the 60-GHz application. In HR SOI substrates the losses are drastically reduced if compared with the bulk silicon technology, consequently, more energy will be provided to the antenna to radiate. The design presented herein makes use of M_{6Z} metal layers for the radiating structure and feeding line.

At the operating frequency the antenna reactance ($Im\{Z_a\}$) must be null and the real part of intrinsic antenna impedance ($Re\{Z_a\}$) must be matched to the LNA input impedance.

Because there are many works about integrated antennas with input impedance $Re\{Z_a\}\approx 50\ \Omega$, we focused on the realization of a radiating structure that presents a good matching with the two-stage LNA (20 Ω in this case).

The integrated antenna is designed taking into account the following guidelines: *i)* the 65-nm SOI CMOS process by ST-Microelectronics has been used, *ii)* the 3D-EM designs did not consider the pad effects since these parasitic effects will be removed by de-embedding during the measurements, *iii)* the knowledge of the effective dielectric constants is necessary to determine the resonant frequency.

The antenna we designed (see Fig. 10) is directly fed by a coplanar strip (CPS) input matching network. The area occupied by the antenna is 0.244 mm^2, which is suited for on chip integration. The 3D polar plot of the antenna gain and the radiation pattern obtained by means of 3D-EM simulations are shown in Fig. 11. In detail, a maximum gain of 3.23 dBi and a return loss (S11) equal to -23.7 dB at 60 GHz, respectively, have been obtained.

In this design, the arm width is carefully selected to reduce the quality factor of resonance and obtain a wider operating bandwidth. A balanced CPS feed line has been selected as input of the dipole antenna, and its length is tuned in order to obtain the wished input impedance. The final 60 GHz fully integrated dipole antenna is realized with following parameters: dipole's length = 760 μm (L_D), width = 22.76 μm (W_D) and 1.1 μm gap between the two dipole's arms. The feeding line's length is of 300 μm (L_{CPS}). The simulated radiation pattern of this antenna is mainly directed toward the SOI substrate, therefore, with a backside metallization the radiation pattern is directed outward the substrate. The distance between radiating arms and the reflector (355 μm ~ $\lambda_g/4$) is close to the optimal distance to prevent TM mode which reduces radiation efficiency. Finally, the dipole antenna has 68.8% of radiation efficiency, with peak directivity of about 3.

V. CONCLUSION

The single-chip integration in 65 nm CMOS SOI technology of a CPS dipole antenna plus a LNA for 60 GHz short-range wireless applications has been presented. Two different LNA architectures are proposed: a three-stage LNA with conventional 50 Ohm input matching and, by relaxing the impedance matching specification due to on-chip co-design of amplifier and antenna, a two-stage LNA. The two-stage LNA achieves similar performance of the three-stage one (gain >22

dB, NF< 5 dB) with a power consumption reduced by 25%. A dipole antenna with CPS feed has been also designed to match the input LNA impedance; it allows for an antenna gain of 3.22 dB at 60 GHz with a limited on-chip area occupation.

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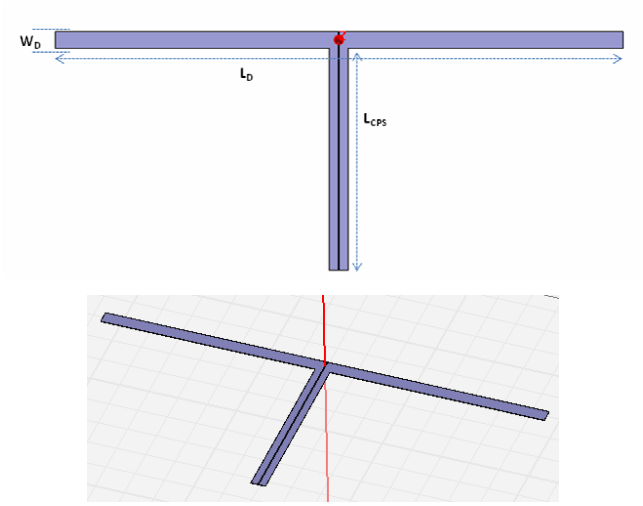

Fig. 10. 60-GHz SOI CMOS CPS dipole antenna a) geometrical parameters and b) design on the 3D-EM simulator.

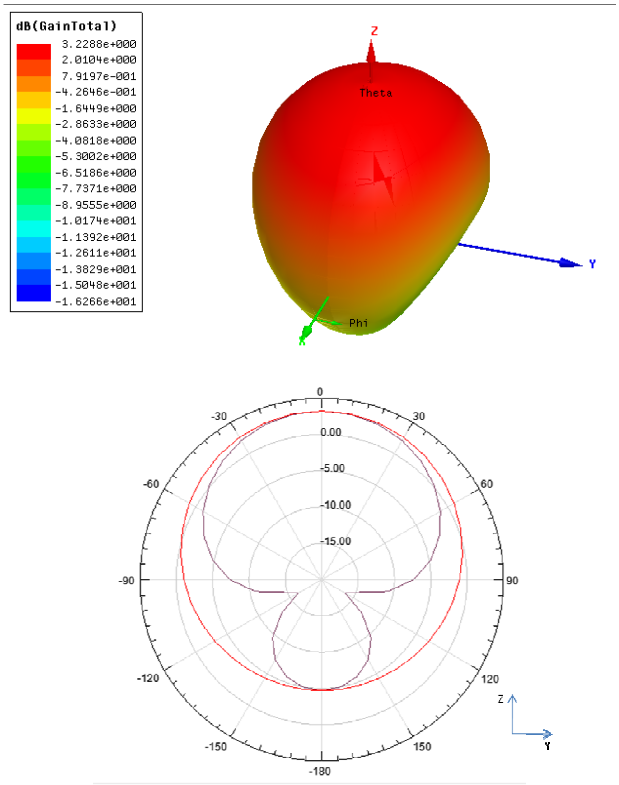

Fig. 11. 60-GHz SOI CMOS CPS dipole antenna: 3D polar plot and radiation pattern.

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