

2.4 GHz 0.18 μ m CMOS Passive Mixer with Integrated Baluns

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Abstract — A 2.4 GHz resistive ring mixer with on-chip baluns is fully integrated in 0.18 μ m IBM7HP process. This mixer exhibits broadband RF impedance matching with return loss better than -10 dB through the RF frequency range from 2 to 6 GHz. The conversion loss of 7.8 dB is achieved at the RF frequency 2.4 GHz. This mixer provides 6 dBm of the input P1dB, and 13.4 dBm of the input IP3 at the operating RF frequency. This mixer is the first reported double-balanced resistive mixer with integrated RF and LO baluns. This mixer has a very compact layout due to the absence of the matching circuits, and is suitable for homodyne and heterodyne transceiver architectures for wireless applications.

Index Terms — Passive mixer, balun, BiCMOS, linearity, conversion loss.

I. INTRODUCTION

The rapid growth of wireless communication services is increasing the demand for low-cost, low-power, and high integration of RF systems. One of key RF building blocks is a mixer where low noise property and high linearity are required. Compared to the traditional “Gilbert Cell” circuit, a passive mixer has the advantage of low Flicker noise and no power consumption, since it operates without DC bias current [1]. A double balanced resistive mixer also exhibits inherent high linearity [2], [3], and it has been shown to be suitable for both homodyne and heterodyne wireless transceivers [4]. Typically, a double-balanced mixer configuration requires single-ended to differential transitions at the RF and LO ports, which are usually implemented off-chip [4]-[9], adding cost, size, and complexity.

In this paper, a 2.4 GHz double-balanced resistive mixer and lumped-element passive baluns were fully integrated in a 0.18 μ m BiCMOS process. This is the first reported double-balanced passive mixer with integrated RF and LO baluns. This mixer is very compact since it does not use any additional passive elements for RF and LO matching. With the RF and LO baluns built on chip, this passive mixer exhibits low conversion loss (CL), excellent linearity, as well as good RF and IF impedance matching, without matching circuits. Low CL, good impedance matching, and high linearity make this mixer suitable for homodyne and heterodyne transceivers for a variety of wireless applications at ISM band. The design process and measurement results of this mixer are elaborated in the following sections.

II. CIRCUIT DESIGN

A schematic of the proposed mixer circuit is shown in Fig. 1. As indicated in Fig. 1, the mixer integrates a resistive CMOS mixer core (Fig. 1 (b)) and a passive balun based on L-C lumped elements (Fig. 1 (a) and (c)). The mixer core employs the topology of a FET ring mixer as published in [2]. The four FET ring mixer presented in Fig. 1(b) provides a double balanced solution with high linearity and good port to port isolation. The L-C lumped-element balun is based on the fact that the insertion phase through a low pass filter lags the insertion phase through a high pass filter [10]. It consists of two capacitors and two inductors, which form a low pass filter and a high pass filter that produce the ± 90 degree phase shifts. It provides the differential RF and LO signals required at the ring mixer inputs.

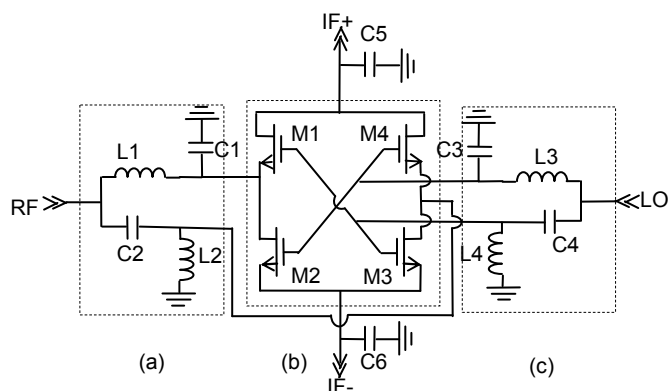


Fig.1 Schematic of the mixer with baluns. (a) RF balun; (b) NMOS ring mixer; (c) LO balun.

The same balun design is reused at the RF and LO ports. Due to the broad-band return loss at the RF, LO, and IF ports, this mixer can be used for heterodyne and homodyne transceiver architectures. As can be seen in Fig.1, the proposed mixer does not have matching at RF and LO ports. The size of the NMOS device is chosen for the best CL, RF impedance matching, and IF matching. The inductors and capacitors of the balun are designed to have a 180-degree phase shift, with minimum loss and equal balanced impedances as well as to improve the RF impedance matching.

Resistive CMOS mixers use the time-varying channel resistance (R) to provide frequency conversion [11]. When the LO power is applied to the gate, it will modulate the depth of the depletion region which varies the channel resistance (R) under the gate, making the transistor behave like a voltage controlled resistor. Ideally, the channel resistance (R) is infinite without any gate bias voltage. When the gate of the device is biased below the threshold voltage, the channel resistance (R) will depend on the V_{gs} linearly:

$$R \approx \frac{L}{W * I_t * n} [n * V_{ds} - V_{gs} + V_T] \quad (1)$$

where $n = 1 + C_{js}/C_{ox}$ (C_{js} is the depletion-region capacitance, and C_{ox} is the oxide capacitance), L is channel length, W is device width, I_t depends on the diffusion of electrons in the channel, V_{ds} is the drain to source voltage, and V_T is thermal voltage [12]. This suggests that an open circuit at the LO ports is needed to provide a maximum gate bias voltage. Without the matching at the LO ports, the mixer sees a high impedance and hence dissipates very little LO power.

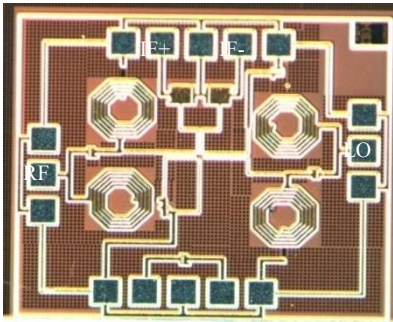


Fig.2 Microphotograph of the mixer with RF and LO baluns.

The simulations were performed using Agilent ADS and the Virtuoso layout tool from Cadence was used for the layout. The mixer is realized with $0.18\mu\text{m}$ 6-metal-layer BiCMOS process from IBM. Fig. 2 shows the microphotograph of the mixer. The chip size is $1.45\text{ mm} \times 1.27\text{ mm}$. The n channel MOSFETs are implemented in multi-fingered gate arrays to reduce gate resistance.

III. RESULTS

The mixer was characterized using a Cascade probe station and several GSGSG probes. The testing results which will be presented were taken under the measurement setting that the LO power level was at 10dBm, and the RF power level was set to -40dBm other than specified otherwise.

The input return loss of each port was measured by using Agilent 8510C vector network analyzer. Fig. 3 and Fig. 4 show the RF, LO and IF return loss of the mixer. The RF

return loss is lower than -10 dB through the frequencies of 2 and 6 GHz, and it is better than -15 dB between 3.4 and 6 GHz. This is the lowest reported RF return loss for a passive mixer, and it is achieved through the optimization of the NMOS device size, with reusing balun reactive elements to enhance the matching. At the LO port, the return loss is above -5 dB from 2 to 6 GHz. This implies a high reflection coefficient at the LO port which leads to a considerable high available V_{gs} , since the LO port is nearly open. At the IF port, the return loss is better than -8 dB at the frequencies below 150 MHz.

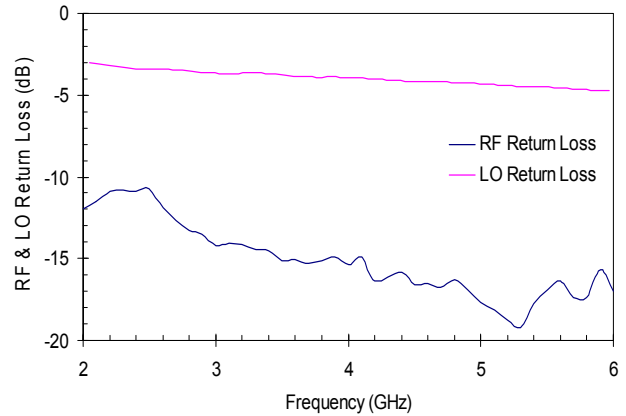


Fig. 3 RF return loss of the mixer, available LO power = 10 dBm.

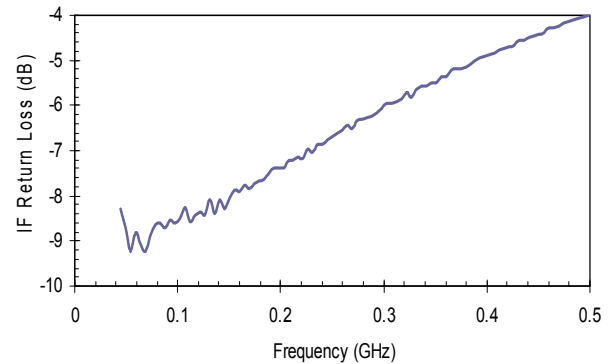


Fig. 4 IF return loss of the mixer, available LO power = 10 dBm.

The result of conversion loss versus the frequency is shown in Fig.5. The CL was measured at a fixed IF frequency of 10 MHz, while both RF and LO frequencies were swept approximately between 2 and 6 GHz. The loss of the cables at different frequencies were measured and compensated for. It can be seen that that the mixer core shows the wide-band performance (CL between 6.3 and 7.1 dB at the RF frequency range from 2 – 6 GHz), and the mixer with baluns shows significant CL increase at the higher frequency. This is due to the increased leakage of the LO to RF and IF ports, which results in lower LO efficiency. Fig. 6 shows mixer with balun

LO-RF and LO-IF isolation, which has -52.7 dB and -30 dB performance at 2.4 GHz respectively, and the similar trend as the CL versus frequency. While this chip was designed for optimum performance at 2.4 GHz, a more broad-band CL performance can be achieved by including LO terminations at the RF port [7], and by including dc bias at the LO port to improve the LO efficiency [7],[8]. The best CL of 7.8 dB is achieved at 2.4 GHz as designed.

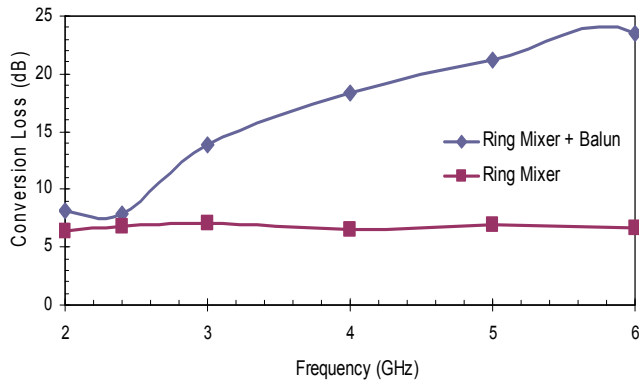


Fig. 5 Conversion loss of the mixer versus RF frequency. IF frequency = 10 MHz, and LO power = 10 dBm.

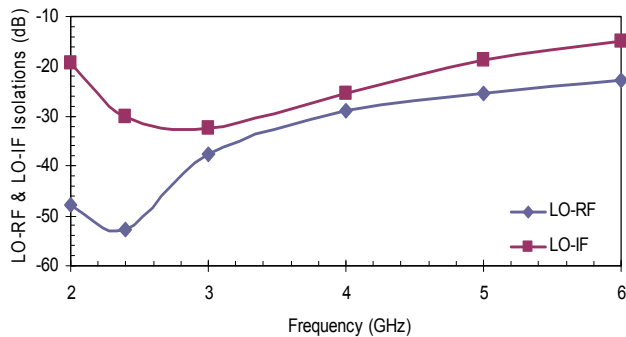


Fig. 6 Measured LO-RF and LO-IF isolation of the mixer with baluns versus RF frequency. IF frequency = 10 MHz, and LO power = 10 dBm.

The important figures of the linearity for a mixer are the 1 dB compression point (P1dB) and the third-order intercept point (IP3). Input P1dB (IP1dB) and input IP3 (IIP3) of the mixer were measured and the results are shown in Table I. The input power range was from -20 dBm to 10 dBm for the IP1dB testing. To determine the IIP3, two tone test was employed. The tone spacing was set at 100 kHz. The IP1dB is 6 dBm and the IIP3 is 13.4 dBm.

The LO-RF and LO-IF isolation were also measured at 2.4 GHz to be -52.7 dB, and -30 dB respectively (Fig. 6). The overall performance of the mixer, including the tester for the ring mixer core itself, is summarized and compared with other published CMOS resistive mixers in Table I.

IV. CONCLUSION

A double balanced resistive mixer with integrated baluns at RF and LO ports were designed, fabricated and measured. The mixer was implemented with 0.18 μ m IBM7HP BiCMOS process. By using the size of the NMOS as a design parameter, the mixer exhibits a broad-band characteristics in RF and IF impedance matching without any matching circuit. The RF return loss is better than -10 dB over the RF frequency range of 2 – 6 GHz. The IF return loss is lower than -8 dB at the IF frequency rang below 150 MHz. At the operating RF frequency of 2.4 GHz, the CL is 7.8 dB at an available LO power level of 10 dBm. The IP1dB and IIP3 of this mixer are 6 dBm and 13.4 dBm, individually. The LO-RF isolation of -52.7 dB, and the LO-IF isolation of -30 dB is achieved at 2.4 GHz. This is the first reported double-balanced passive resistive mixer with integrated RF and LO baluns, with the best RF return loss reported to date. This compact integrated design is suitable for low power, high linearity wireless transceiver.

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TABLE I
SUMMARIZED PERFORMANCES OF THIS MIXER AND ITS COMPARISON WITH PREVIOUSLY PUBLISHED DATA

	This work		[6]	[7]	[8]	[9]	[10]
	Mixer Core	Mixer + Balun					
Technology	BiCMOS 0.18 μ m	BiCMOS 0.18 μ m	BiCMOS 0.25 μ m	CMOS 130nm	CMOS 130nm	CMOS 0.25 μ m	CMOS 0.18 μ m
Topology	Double balanced	Double balanced	Double balanced	Double balanced	Double balanced	Double balanced	Double balanced
Matching Circuit	No	No	RF and LO	No	No	RF and LO	RF and IF
On-Chip Balun	No	Yes	No	No	No	No	No
RF* Frequency (GHz)	2 – 6	1.8 – 2.6	1.8	2 – 3	5 – 6	2 – 9	1 – 11
IF Frequency (MHz)	10	10	170	~0	2500	0.1	500
LO Power (dBm)	10	10	14	0	0	10	9
Gate bias (V)	0	0	0	0.33	0.3	0.45	—
CL (dB)	6.8 @ 2.4 GHz	7.8 @ 2.4 GHz	5.8**	5.6**	6**	6.4**	6.5**
IP1dB (dBm)	7 @ 2.4 GHz	6 @ 2.4 GHz	10	0 @ 2.5 GHz	—	4 – 6.5	4 – 6***
IIP3 (dBm)	14 @ 2.4 GHz	13.4 @ 2.4 GHz	19.5	10 @ 2.5 GHz	10 – 14	11.4 – 14.3	9 – 13***
LO-RF Isolation (dB)	-58 @ 2.4 GHz	-52.7 @ 2.4 GHz	—	-48	-45	-51	-36
LO-IF Isolation (dB)	-20 @ 2.4 GHz	-30 @ 2.4 GHz	43	-52	-44	-36	—
RF Return Loss (dB)	-6 – -8 @ 2 – 6 GHz	-19.3 – -10.3 @ 2 – 6 GHz	—	—	< -15	-18 – -8.6	-32 – -4
IF Return Loss (dB)	< -6.9 @ DC – 1 GHz	< -8 @ DC – 150 MHz	—	—	—	< -8 @ DC – 135 MHz	—
Power Consumption (mW)	0	0	0	0	0	0	3

* Estimated 3dB bandwidth based on the data in Fig.5.

** Lowest conversion loss (CL) versus RF frequency.

*** IP1dB and IIP3 were measured between 1 and 12 GHz.

— Not specified.

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